6533 103518

# SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 9-08-03 Serial # 09/975,257 Priority Application Date 10-12-01

Your Name David Hogans Examiner # 79069

AU 2813 Phone 305-3361 Room CP4 4D14

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

**If submitting more than one search, please prioritize in order of need.**

**The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.**

09-10-03 A09:55 IN

Where have you ~~searched~~ so far on this case?

Circle: (NSPT) (DWPI) (RPO Abs) (JPO Abs) IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. 6,528,433 to Gartner et al.

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ✓ Other _____

Secondary Refs ___ Foreign Patents ✓

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Please search clms 1, 10 & 19

novelty & clm 1 measuring the thickness of an oxide layer (or an oxidized layer) to determine nitrogen content of a gate oxide layer to see if there is too much (or too little) nitrogen (i.e. exceeds predetermined value)

clm 10: using estimated gate oxide thickness to determine change in thickness

Staff Use Only

Searcher: HARRISON

Searcher Phone: 306-5429

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 9-15-03

Date Completed: 9-15-03

Searcher Prep/Rev Time: 90

Online Time: 70

Type of Search

Structure (#)___

Bibliographic X

Litigation___

Fulltext___

Patent Family___

Other___

Vendors

STN X

Dialog___

Questel/Orbit___

Lexis-Nexis___

WWW/Internet___

Other___

09/975,257

9/15/03

```
     FILE 'REGISTRY' ENTERED AT 13:32:01 ON 15 SEP 2003
L1        51376 SEA ABB=ON  PLU=ON  N/ELF

     FILE 'HCAPLUS' ENTERED AT 13:32:25 ON 15 SEP 2003
L2          320 SEA ABB=ON  PLU=ON  L1(L)GATE AND L1(L)OXIDE
L3        32906 SEA ABB=ON  PLU=ON  ("N" OR NITROGEN)(2A)CONCENTRATION
L4       118493 SEA ABB=ON  PLU=ON  CONCENTRATION(4A)(CORRELAT? OR FUNCTION OR
                PROPORTIONAL OR RELATED)
L5        13899 SEA ABB=ON  PLU=ON  THICKNESS(4A)(CORRELAT? OR FUNCTION OR
                PROPORTIONAL OR RELATED)
L6            8 SEA ABB=ON  PLU=ON  L3 AND L4 AND L5
L7            0 SEA ABB=ON  PLU=ON  L2 AND L3 AND L4
L8            0 SEA ABB=ON  PLU=ON  L2 AND L3 AND L5
L9            0 SEA ABB=ON  PLU=ON  L2 AND L4 AND L5
L10          33 SEA ABB=ON  PLU=ON  L2 AND CONCENTRATION
                D L6 ALL TOT
L*** DEL    105 S L2 AND (REOXID? OR OXIDAT? OR OXIDIS? OR OXODIZ?)
L11         114 SEA ABB=ON  PLU=ON  L2 AND (REOXID? OR OXIDAT? OR OXIDIS? OR
                OXIDIZ?)
L12          46 SEA ABB=ON  PLU=ON  L11 AND THICKNESS
L13          11 SEA ABB=ON  PLU=ON  L10 AND L11
                D ALL TOT
L14           1 SEA ABB=ON  PLU=ON  L12 AND CALC########
                D ALL

     FILE 'STNGUIDE' ENTERED AT 13:38:05 ON 15 SEP 2003

     FILE 'HCAPLUS' ENTERED AT 13:44:20 ON 15 SEP 2003
L15           4 SEA ABB=ON  PLU=ON  L2 AND PREDICT######
                D ALL TOT
L16        3492 SEA ABB=ON  PLU=ON  THICKNESS(3A)CONCENTRATION
L17          78 SEA ABB=ON  PLU=ON  (L2 OR L3) AND L16
L18           4 SEA ABB=ON  PLU=ON  L17 AND CALCULAT######
L19           1 SEA ABB=ON  PLU=ON  L17 AND ?MONITOR?
L20           0 SEA ABB=ON  PLU=ON  L17 AND REGRESS#######
L21           9 SEA ABB=ON  PLU=ON  L17 AND FUNCTION
L22           3 SEA ABB=ON  PLU=ON  L17 AND CORRELAT########
L23          14 SEA ABB=ON  PLU=ON  (L18 OR L19 OR L20 OR L21 OR L22) NOT L15
                D ALL TOT
L24           1 SEA ABB=ON  PLU=ON  PLASMA NITRIDATION OPTIMIZATION
                D RE
                D ALL
L25           1 SEA ABB=ON  PLU=ON  PLASMA NITRIDATION OPTIMIZATION
                D ALL
L26             SEL PLU=ON  L25 1- RE :      14 TERMS
L27        1160 SEA ABB=ON  PLU=ON  L26
L28         172 SEA ABB=ON  PLU=ON  L27 AND THICKNESS
L29           1 SEA ABB=ON  PLU=ON  L28 AND PREDICT########
                D ALL
L30          11 SEA ABB=ON  PLU=ON  L28 AND FUNCTION
                D ALL TOT
L31             SEL PLU=ON  L25 1- RAU :      13 TERMS
L32        1452 SEA ABB=ON  PLU=ON  L31/AU
L33       17400 SEA ABB=ON  PLU=ON  L31
L34         817 SEA ABB=ON  PLU=ON  L33 AND THICKNESS
                S L34 AND N/ELF

     FILE 'REGISTRY' ENTERED AT 14:34:26 ON 15 SEP 2003
L35       51376 SEA ABB=ON  PLU=ON  N/ELF

     FILE 'HCAPLUS' ENTERED AT 14:34:27 ON 15 SEP 2003
L36      361677 SEA ABB=ON  PLU=ON  L35
L37          72 SEA ABB=ON  PLU=ON  L34 AND L36
L38           7 SEA ABB=ON  PLU=ON  L37 AND FUNCTION
L39           5 SEA ABB=ON  PLU=ON  L37 AND CORRELAT########
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L40          72 SEA ABB=ON  PLU=ON  L37 AND THICKNESS
L41          11 SEA ABB=ON  PLU=ON  (L38 OR L39)
                D ALL TOT
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     FILE 'HCAPLUS, WPIX' ENTERED AT 11:13:46 ON 15 SEP 2003
L54            2 SEA ABB=ON  PLU=ON  US6528433/PN
L55              SEL PLU=ON  L54 1- RN IC :      12 TERMS
L56       926915 SEA ABB=ON  PLU=ON  L55
L57            2 SEA ABB=ON  PLU=ON  L54 AND L56
                 D ALL HITSTR
                 D MAX 2

     FILE 'DPCI' ENTERED AT 11:15:11 ON 15 SEP 2003
L58            1 SEA ABB=ON  PLU=ON  (DE 10029286 OR US 6528433)/PN
L59            0 SEA ABB=ON  PLU=ON  (DE 10029286 OR US 6528433)/PN.D
L60            4 SEA ABB=ON  PLU=ON  (DE 10029286 OR US 6528433)/PN.G
L61            5 SEA ABB=ON  PLU=ON  (L58 OR L59 OR L60)
L62              SEL PLU=ON  L61 1- PRN :       7 TERMS
L63              SEL PLU=ON  L61 1- PN.D :      69 TERMS
L64              SEL PLU=ON  L61 1- PN.G :     118 TERMS
L65           54 SEA ABB=ON  PLU=ON  L63/PN
L66          111 SEA ABB=ON  PLU=ON  L64/PN
L67          233 SEA ABB=ON  PLU=ON  L63/PN.G
L68          704 SEA ABB=ON  PLU=ON  L64/PN.G
L69          376 SEA ABB=ON  PLU=ON  L64/PN.D
L70         1258 SEA ABB=ON  PLU=ON  (L65 OR L66 OR L67 OR L68 OR L69)
L71         1659 SEA ABB=ON  PLU=ON  L63
L72          704 SEA ABB=ON  PLU=ON  L64
L73         2675 SEA ABB=ON  PLU=ON  (L70 OR L71 OR L72)
L74           25 SEA ABB=ON  PLU=ON  L73 AND MEASUR#########
L75          163 SEA ABB=ON  PLU=ON  L73 AND THICK##########
L76          600 SEA ABB=ON  PLU=ON  L73 AND GATE
L77          656 SEA ABB=ON  PLU=ON  L73 AND OXID######
L78          341 SEA ABB=ON  PLU=ON  L73 AND OXID######(2A)(FILM OR LAYER)
L79          263 SEA ABB=ON  PLU=ON  L76 AND L77
L80          464 SEA ABB=ON  PLU=ON  L73 AND ("N" OR NITRID? OR NITROGEN?)
L81          308 SEA ABB=ON  PLU=ON  (L75 OR L76 OR L77 OR L78) AND L80
L82          818 SEA ABB=ON  PLU=ON  (L74 OR L75) OR (L78 OR L79 OR L80 OR L81)

L83              SEL PLU=ON  L74 1- PRN :       42 TERMS
L84              SEL PLU=ON  L61 1- IC :        18 TERMS
L85        55663 SEA ABB=ON  PLU=ON  L84
L86          454 SEA ABB=ON  PLU=ON  L82 AND L85
L87              SEL PLU=ON  L86 1- PRN :      619 TERMS
L88              SEL PLU=ON  L75 1- PRN :      221 TERMS

     FILE 'WPIX, HCAPLUS, JAPIO' ENTERED AT 11:24:16 ON 15 SEP 2003
L89           11 SEA ABB=ON  PLU=ON  L62
L90       296398 SEA ABB=ON  PLU=ON  L84
L91          454 SEA ABB=ON  PLU=ON  L88
L92         1279 SEA ABB=ON  PLU=ON  L87
                 D L89 TI 1-11
                 D L89 1-6 MAX
                 D L89 7-11 ALL
L93         1028 SEA ABB=ON  PLU=ON  L90 AND (L91 OR L92)
L94          407 SEA ABB=ON  PLU=ON  L93 AND THICK#########
L95          280 SEA ABB=ON  PLU=ON  L94 AND ("N" OR NITROGEN? OR NITRID?)
L96          204 SEA ABB=ON  PLU=ON  L95 AND GATE
L97           21 SEA ABB=ON  PLU=ON  L96 AND (EXCEED? OR VALUE? OR PRE OR
                 PREDETERMIN? OR PREESTABLISH? OR TARGET? OR GOAL? OR SET OR
                 SETPOINT)
L98            2 SEA ABB=ON  PLU=ON  L96 AND MEASUR?
L99            1 SEA ABB=ON  PLU=ON  L96 AND CALCULAT?
L100           3 SEA ABB=ON  PLU=ON  L96 AND (DELTA OR CHANG######)
L101           8 SEA ABB=ON  PLU=ON  L96 AND (ESTIMAT######## OR APPROX#########
                 )
L102           6 SEA ABB=ON  PLU=ON  L95 AND (EXCESS? OR EXCEED? OR TOO(W)
                 MUCH)
L103         233 SEA ABB=ON  PLU=ON  L95 AND THICKNESS
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L104          30 SEA ABB=ON  PLU=ON  L94 AND ("N" OR NITROGEN? OR NITRID?)(2A)(C
                 ONC OR CONCN OR CONCD OR CONCENTRAT? OR AMOUNT OR WT OR WEIGHT
                 OR ATOMIC)
L105      324191 SEA ABB=ON  PLU=ON  (SION OR OXYNITRID? OR OXID######)(2A)(FILM
                  OR LAYER)
L106      390095 SEA ABB=ON  PLU=ON  THICKNESS(6A)(FILM OR LAYER)
L107       41833 SEA ABB=ON  PLU=ON  L105 AND L106
L108        5033 SEA ABB=ON  PLU=ON  L107 AND MEASUR?
L109        1383 SEA ABB=ON  PLU=ON  L107 AND CALCULAT?
L110        2017 SEA ABB=ON  PLU=ON  L107 AND (APPROXIMAT? OR ESTIMAT?)
L111        1029 SEA ABB=ON  PLU=ON  L108 AND (L109 OR L110)
L112      105261 SEA ABB=ON  PLU=ON  ("N" OR NITROGEN? OR NITRID?)(2A)(CONC OR
                 CONCN OR CONCD OR CONCENTRAT? OR AMOUNT OR WT OR WEIGHT OR
                 ATOMIC)
L113          60 SEA ABB=ON  PLU=ON  (L108 OR L109 OR L110) AND L112
L114         127 SEA ABB=ON  PLU=ON  (L97 OR L98 OR L99 OR L100 OR L101 OR
                 L102) OR L104 OR L113
L115         125 SEA ABB=ON  PLU=ON  L114 NOT L89
L116           0 SEA ABB=ON  PLU=ON  L115 AND CYPRESS?/CS,PA
L117           1 SEA ABB=ON  PLU=ON  L115 AND (NARAYANAN? OR RAMKUMAR?)/AU,IN
                 D TI
                 D MAX
L118           2 SEA ABB=ON  PLU=ON  US2003073255/PN
L119           3 SEA ABB=ON  PLU=ON  (L117 OR L118)
L120             SEL PLU=ON  L119 1- IC MC :      17 TERMS
L121      145462 SEA ABB=ON  PLU=ON  L120
L122          35 SEA ABB=ON  PLU=ON  L115 AND L121
L123          34 SEA ABB=ON  PLU=ON  L122 NOT (L117 OR L89)
                 D TI 1-34
                 D MAX 1-31
                 D ALL 32-34
L124          77 SEA ABB=ON  PLU=ON  L115 AND GATE
L125           5 SEA ABB=ON  PLU=ON  L115 AND SAMPL#####
L126          14 SEA ABB=ON  PLU=ON  L115 AND (CHANG##### OR DELTA)
L127         116 SEA ABB=ON  PLU=ON  L115 AND THICKNESS
L128           1 SEA ABB=ON  PLU=ON  L115 AND (SELF OR ITSELF)
L129           2 SEA ABB=ON  PLU=ON  L115 AND MONITOR########
L130           0 SEA ABB=ON  PLU=ON  L115 AND CALIBRAT?
L131           0 SEA ABB=ON  PLU=ON  L115 AND REGRESS######
L132           0 SEA ABB=ON  PLU=ON  L115 AND LEAST SQUARE
L133          10 SEA ABB=ON  PLU=ON  L115 AND COMPAR########
L134          62 SEA ABB=ON  PLU=ON  L115 AND METHOD
L135          59 SEA ABB=ON  PLU=ON  L115 AND PROCESS
L136          13 SEA ABB=ON  PLU=ON  L115 AND (ULTRA THIN OR ULTRATHIN#####)
L137          46 SEA ABB=ON  PLU=ON  L122 OR L117 OR L89
L138          16 SEA ABB=ON  PLU=ON  (L125 OR L126)
L139          12 SEA ABB=ON  PLU=ON  (L128 OR L129 OR L130 OR L131 OR L132 OR
                 L133)
L140          35 SEA ABB=ON  PLU=ON  L138 OR L139 OR L136
L141          68 SEA ABB=ON  PLU=ON  L124 AND L127
L142          64 SEA ABB=ON  PLU=ON  L124 AND (L134 OR L135)
L143          84 SEA ABB=ON  PLU=ON  L127 AND (L134 OR L135)
L144          55 SEA ABB=ON  PLU=ON  L141 AND L142
L145          81 SEA ABB=ON  PLU=ON  L140 OR L144
L146          53 SEA ABB=ON  PLU=ON  L145 NOT L137
L147          53 SEA ABB=ON  PLU=ON  L146 AND THICKNESS
                 D TI 1-53
                 D MAX 1-15
                 D ALL 16-53
L148        1484 SEA ABB=ON  PLU=ON  (L91 OR L92 OR L93 OR L94 OR L95 OR L96)
L149          57 SEA ABB=ON  PLU=ON  L148 AND COMPAR?
L150          39 SEA ABB=ON  PLU=ON  L149 AND THICK########
L151          34 SEA ABB=ON  PLU=ON  L150 NOT (L145 OR L137)
```

L123 ANSWER 30 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1992-303736 [37] WPIX
CR 1992-230168 [28]
DNN N1993-260686 DNC C1993-149242
TI Mfr. of semiconductor, esp. MOS devices - by forming first and second oxide films by **nitridation**, the **thickness** of each being independently **set** and the variations in oxide **thickness** being decreased.
DC L03 U11 U13
IN NAKATA, H
PA (NIDE) NEC CORP
CYC 2
PI JP 04208570 A 19920730 (199237)* 8p H01L029-784
US 5254489 A 19931019 (199343)B 14p H01L021-265 <--
ADT JP 04208570 A JP 1990-340916 19901130; US 5254489 A US 1991-779078 19911018
PRAI **JP 1990-340916 19901130; JP 1990-280393 19901018**
IC ICM **H01L021-265**; H01L029-784
ICS H01L027-088; **H01L029-788**; **H01L029-792**
AB US 5254489 A UPAB: 19931207 ABEQ treated as Basic
Mfr. of a semiconductor device comprises: (a) forming an element- and an element isolating (2)- region on a first conductivity substrate (1): (b) forming an oxide(s), **gate** insulating film in the element region: (c) annealing in N2 or NH3 to nitrify the above oxide; (d) thermally oxidising the nitrified film (6); (e) removing pt. of the nitrified film and forming a second oxide film serving as a **gate** insulating film in the removed area; and (f) forming a polysilicon film **gate** electrode (10) on the first and second oxide film.

Pref. method comprises following steps (a)-(f), then: (g) forming a diffusion source and drain in the substrate; (h) forming an insulating interlayer (12) on the oxide, nitrified and the **gate** electrode; (i) forming contact holes (12a) in the interlayer on the diffusion layers and forming wiring electrodes (13) on the interlayer; and (j) forming a protective, covering insulating (14) film on the interlayer and the electrode.

USE/ADVANTAGE - Used to mfr. a MOS semiconductor device. The **thickness** of the first **gate** oxide film can be **set** independently to that of one formed in a later step. Variations in the **gate** oxide film **thickness** are decreased. (First major country equivalent to J04154162-A, J04208570-A) Dwg.3a-h/5
AB JP 04208570 A UPAB: 19971125
Dwg.1f/5
Dwg.1f/5
FS CPI EPI
FA AB; GI

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1994:618803 HCAPLUS
DN 121:218803
TI Rapid thermal oxidation of silicon in N2O between 800 and 1200°C: incorporated nitrogen and interfacial roughness
AU Green, M. L.; Brasen, D.; Evans-Lutterodt, K. W.; Feldman, L. C.; Krisch, K.; Lennard, W.; Tang, H.-T.; Manchanda, L.; Tang, M.-T.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO Applied Physics Letters (1994), 65(7), 848-50
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB Oxynitrides can suppress the diffusion of boron from the polycryst. silicon gate electrode to the channel region of an ultralarge scale integrated device, and are therefore important potential substrates for thin SiO2 gates. Direct oxynitridation of Si in N2O is a simple and manufacturable N incorporation scheme. Authors used rapid thermal oxidn. to grow O2- and N2O-oxides of technol. importance (~10 nm thick) in the temp. range 800-1200°. Accurate measurements of the N content of the N2O-oxides were made using nuclear reaction anal. N content increases linearly with oxidn. temp., but is in general small. A 1000°C N2O-oxide contains about 7 × 1014 N/cm2, or the equiv. of about one monolayer of N on Si (100). Nonetheless, this small amt. of N can retard boron penetration through the dielec. by two orders of magnitude as compared to O2-oxides. The N is contained in a Si-O-N phase within about 1.5 nm of the Si/SiO2 interface, and can be pushed away from the interface by O2-reoxidn. Authors measured Si/SiO2 interfacial roughness by x-ray reflectometry, and found that it decreases with increasing oxidn. temp. for both O2- and N2O-oxides, although the N2O-oxides are smoother. The enhanced smoothness of N2O-oxides is greater the greater the N content. N2O-oxides are promising candidates for thin ultralarge scale integrated circuit gate dielecs.

# STIC Search Report
## EIC 2800

STIC Database Tracking Number: 103518

| | |
|---|---|
| **TO: David Hogans**<br>**Location: 4D14**<br>**Art Unit: 2813**<br>**9/15/03**<br><br>**Case Serial Number: 09/975,257** | **From: Jeff Harrison**<br>**Location: STIC-EIC2800**<br>**CP4-9C18**<br>**Phone: 306-5429**<br><br>**Email: harrison, jeff** |

## Search Notes

Examiner Hogans;

Re: Nitrogen concentration, gate-oxide thicknesses

Attached are edited search results from the patent and NPL literature, mostly Chemical Abstracts, and from a citation search in Derwent Patents Citation Index based on the close patents you previously found.

I tagged some that looked in the ballpark.

Based on this, if you have questions or would like a refocused search, please contact me.

Thanks,
Jeff
Jeff Harrison
Team Leader, STIC-EIC2800
CP4-9C18, 703-306-5429

15sep03 10:55:38 User259284 Session D2382.1

File 2:INSPEC 1969-2003/Sep W1

*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

| Set | Items | Description |
|---|---|---|
| S1 | 37906 | 'THICKNESS MEASUREMENT' OR 'SPATIAL VARIABLES MEASUREMENT' OR 'THICKNESS CONTROL' OR R7:R8 |
| S2 | 291 | S1 AND GATE |
| S3 | 66 | S2 AND CI=O |
| S4 | 14 | S3 AND CI=N |
| S5 | 5 | THICKNESS? AND GATE?? AND CI=N AND CI=O AND (MEASUR? OR MONITOR? OR DETERMIN?)/TI |
| S6 | 4 | S5 NOT S4 |

L89 ANSWER 2 OF 11 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1998-193923 [17] WPIX
DNN N1998-153447 DNC C1998-062161
TI Ultra-thin silicon oxynitride dielectric layer production - giving nitrogen concentration peaks near each interface surface which is effective for inhibiting diffusion of dopants from surfaces in contact.
DC L03 U11 U12 U13 U14
IN HAO, M; OGLE, R B; WRISTERS, D
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 20

| | | | | | | |
|---|---|---|---|---|---|---|
| PI | WO 9810464 | A1 | 19980312 (199817)* | EN | 24p | H01L021-28 |
| | EP 928497 | A1 | 19990714 (199932) | EN | | H01L021-28 |
| | R: DE FR GB NL | | | | | |
| | US 5939763 | A | 19990817 (199939) | | | H01L029-78 |
| | KR 2000035980 | A | 20000626 (200111) | | | H01L021-28 |
| | JP 2001502115 | W | 20010213 (200112) | | 27p | H01L021-318 |
| | US 6245689 | B1 | 20010612 (200135) | | | H01L021-31 |

AB WO 9810464 A UPAB: 19980428
Making a thin dielectric layer on a clean surface of a silicon (Si) substrate comprises: (a) placing the Si substrate (8) in an annealing chamber; (b) providing a first pressure of nitric oxide gas in the annealing chamber; (c) annealing the substrate at a first elevated temperature for a first period of time; (d) removing the nitric oxide gas from the annealing chamber; (e) providing a second pressure of oxidising gas in the annealing chamber; and (f) annealing the substrate at a second elevated temperature for a second period of time, thereby providing an oxynitride dielectric layer (10) on the clean surface (11) of the Si substrate. The oxynitride dielectric layer has a first peak (24) in the nitrogen concentration near the interface (16) with the Si substrate, and a second peak (22) in the nitrogen concentration near the surface (14) of the oxynitride dielectric layer. The oxynitride layer is effective for inhibiting the diffusion of dopants from surfaces in contact with it.

Also claimed are: (i) a Si semiconductor wafer having at least one integrated circuit in it, and having a thin dielectric layer fabricated as above; (ii) an integrated circuit device in a Si wafer.

USE - Used in the fabrication of semiconductor integrated circuit devices, especially for ultra-thin dielectric layers as gate or tunnel oxides in e.g. MOS transistors and floating gate memory elements.

ADVANTAGE - The provides precise thickness control, improved interface structure, low density of electron traps and impedes diffusion of dopant impurity from/to the dielectric and substrate. The process can be readily incorporated into existing manufacturing processes for little added cost.

2C,2D,2E/5

FS CPI EPI

L89 ANSWER 6 OF 11 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1994-233900 [28] WPIX
DNN N1994-184984 DNC C1994-106374
TI Controlling gate oxide thickness in semiconductor device mfr. - uses selective nitrogen implantation to control subsequent oxidn. growth rate.
DC L03 U11
IN DOYLE, B S; PHILIPOSSIAN, A; SOLEIMANI, H R
PA (DIGI) DIGITAL EQUIP CORP
CYC 5
PI US 5330920 A 19940719 (199428)* 5p H01L021-265
EP 631308 A2 19941228 (199505) EN 5p H01L021-82
R: DE FR GB IT
EP 631308 A3 19960612 (199632) H01L021-265
EP 631308 B1 19981125 (199851) EN H01L021-82
R: DE FR GB IT
DE 69414764 E 19990107 (199907) H01L021-82
AB US 5330920 A UPAB: 19940831
Controlling gate oxide thickness is semiconductor device mfr. comprises forming a sacrificial gate oxide at selected locations on a semiconductor substrate (10), implanting N ions into the select locations through the oxide, thermally annealing to aid N pile-up at the substrate surface, and removing the sacrificial oxide. A gate oxide is thermally grown on the substrate (26) and will be thinner over the N-implanted regions (30) than elsewhere (34).

The substrate is Si, oxide layers are formed and removed prior to the sacrificial layer, N ions are implanted at 10 x power 13-10 x power 17 ions cm-2, and annealing is at 800-1100 deg.C for 1-90 minutes. The gate oxide is formed under dry O2 at 800-1000 deg.C for 5-20 minutes.

USE/ADVANTAGE - For semiconductor device prodn. The method of controlling gate oxide thickness is simple and rapid, mask contamination is avoided, and thick gate oxide layers may be applied over I/O drivers to avoid early TDDB failure.

Dwg.6/6
FS CPI EPI
FA AB
MC CPI: L04-C02B; L04-C07; L04-C12A

L123 ANSWER 4 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2003-156108 [15] WPIX
CR 2002-681294 [73]
DNN N2003-123205 DNC C2003-040464
TI Formation of silicon **nitride gate** insulators and silicon dioxide **gate** insulators, for digital and analog transistors, involves forming **gate** insulators from silicon **nitride** layer and new silicon dioxide layer.
DC L03 U11 U12 U13
IN KAMATH, A; MIRABEDINI, M; PATEL, R
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 2002151188 A1 20021017 (200315)* 12p H01L021-31 <--
US 6562729 B2 20030513 (200335) H01L021-31 <--
ADT US 2002151188 A1 Div ex US 2000-723516 20001128, US 2002-171700 20020614;
US 6562729 B2 Div ex US 2000-723516 20001128, US 2002-171700 20020614
FDT US 2002151188 A1 Div ex US 6436845; US 6562729 B2 Div ex US 6436845
PRAI **US 2000-723516 20001128**; US 2002-171700 20020614
IC ICM **H01L021-31**
ICS **H01L021-469**
AB US2002151188 A UPAB: 20030603
NOVELTY - Silicon **nitride gate** insulators and silicon oxide **gate** insulators are formed by forming a silicon **nitride** layer on an exposed silicon substrate, removing an initial silicon dioxide layer, forming a new silicon dioxide layer, and forming **gate** insulators from the silicon **nitride** layer and from the new silicon dioxide layer.

DETAILED DESCRIPTION - Formation of silicon **nitride gate** insulators (36) for a first type of transistor of an integrated circuit (IC) formed on a silicon substrate (26) while forming silicon oxide **gate** insulators (46) for a second different type of transistor of the IC, comprises exposing a first area of the silicon substrate in which the **gate** insulators of the first transistors are to be formed. An initial silicon dioxide layer is formed on the silicon substrate in a second area in which the **gate** insulators of the second transistors are to be formed. The first and second areas are separated from one another. A silicon **nitride** layer is formed on the exposed silicon substrate in the first area, while the initial silicon dioxide layer inhibits the formation of silicon **nitride** on the second area. The initial silicon dioxide layer is removed after the silicon **nitride** layer has been formed. A new silicon dioxide layer is formed into the silicon substrate of the second area exposed after removing the initial layer of silicon dioxide. The **gate** insulators for the first transistors are formed from the silicon **nitride** layer. The **gate** insulators for the second transistors are formed from the new layer of silicon dioxide.

An INDEPENDENT CLAIM is included for a hybrid IC containing high frequency digital switching transistors (22) and analog linear response transistors (24) formed on a silicon substrate.

USE - For digital and analog transistors.

ADVANTAGE - The process offers an enhanced resistance to direct quantum mechanical tunneling of electrons and holes between the **gate** and the channel, to diminish leakage current. It achieves a greater differential in the relative **thickness** of the **gate** insulators of the digital transistors and the analog transistors.

DESCRIPTION OF DRAWING(S) - The figure shows a simplified, broken, cross-sectional view of a portion of the hybrid integrated circuit.

Digital switching transistors 22
Analog linear response transistors 24
Substrate 26
Silicon **nitride gate** insulators 36
Silicon oxide **gate** insulators 46
Dwg.1/9
TECH US 2002151188 A1UPTX: 20030303

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The silicon **nitride** layer is used as an oxidation barrier to inhibit the formation of silicon dioxide on the first area while forming the new layer of silicon dioxide in the second area. A silicon dioxide interface is created between the silicon **nitride** and the silicon substrate in the first area while forming the new silicon dioxide layer in the second area. The silicon dioxide interface is limited to a **thickness** less than that of the silicon **nitride** at the first area. The silicon of the exposed substrate is oxidized in the second area to create the new layer of silicon dioxide. The silicon **nitride** layer in the first area is oxidized while forming the new layer of silicon dioxide in the second area. Traps and defects in the silicon **nitride** layer created when forming the silicon **nitride** layer, are removed by oxidizing the silicon **nitride** layer. Silicon **nitride** is deposited by chemical vapor deposition to form the silicon **nitride** layer in the first area. The chemical vapor deposition of silicon **nitride** is applied to the silicon dioxide in the second area while the silicon **nitride** is deposited by chemical vapor deposition in the first area. The silicon **nitride** layer is formed to have a smaller **thickness** than the **thickness** the new layer of silicon dioxide. The initial silicon dioxide layer is etched in hydrofluoric acid to remove the initial silicon dioxide layer from the second area. A mask material is applied to the initial silicon dioxide layer on the second area after the initial layer of silicon dioxide has been formed on the first area. The initial silicon dioxide layer is etched on the first area into a layer having a lesser **thickness** than the **thickness** of the initial layer of silicon dioxide on the second area while the mask material remains applied to the initial silicon dioxide layer on the second area. The mask material is removed from the initial layer of silicon dioxide on the second area while the lesser **thickness** layer of silicon dioxide remains on the first area. The lesser **thickness** silicon dioxide layer on the first area is etched to expose the first area of the silicon substrate. The initial silicon dioxide layer on the second area is simultaneously etched into a lesser **thickness** prior to forming the layer of silicon **nitride** on the exposed first area of the silicon substrate. The silicon dioxide layers are bathed in hydrofluoric acid to etch the silicon dioxide layers. The silicon substrate in the first area is protected beneath the lesser **thickness** silicon dioxide from the one of the hydrogen sulfide oxidizer or the plasma asher in combination with the hydrogen sulfide oxidizer. The **gate** insulators for the digital and analog transistors are **approximately** simultaneously formed during the formation of the IC. The silicon **nitride gate** insulator of each digital transistor is formed to a **thickness** of 10-30 Angstrom, and the silicon dioxide **gate** insulator of each analog transistor is formed to a **thickness** of at least 60 Angstrom. The silicon **nitride** is formed to contain at least 20% **nitrogen**.
Preferred Component: The first transistors are high frequency digital switching transistors, and the second transistors are analog linear response transistors.

FS CPI EPI

FA AB; GI

MC CPI: L03-G04A; **L04-C12A**; L04-C12B; L04-E01
EPI: **U11-C05B5**; **U11-C05F1**; U12-D01A; U12-D02A; U13-C09

L123 ANSWER 6 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-642040 [69] WPIX
DNN N2002-507439 DNC C2002-181297
TI Formation of metal oxide semiconductor transistor (MOST) gate dielectric **layer** involves annealing **oxynitride layer** in nitrous **oxide**.
DC L03 U11
IN GRIDER, D T
PA (TEXI) TEXAS INSTR INC; (GRID-I) GRIDER D T
CYC 2
PI US 2002072177 A1 20020613 (200269)* 6p H01L021-336
JP 2002198531 A 20020712 (200269) 6p H01L029-78
ADT US 2002072177 A1 Provisional US 2000-241673P 20001019, US 2001-967044 20010928; JP 2002198531 A JP 2001-321458 20011019
PRAI US 2000-241673P 20001019; US 2001-967044 20010928
IC ICM H01L021-336; H01L029-78
ICS H01L021-318; H01L021-76
AB US2002072177 A UPAB: 20021026
NOVELTY - A metal oxide semiconductor (MOS) transistor gate dielectric layer is formed by forming an **oxide layer** on a semiconductor substrate; exposing the **oxide layer** to a high-density nitrogen plasma to incorporate nitrogen into the **oxide layer** and convert it to an **oxynitride layer**; and annealing the **oxynitride layer** in nitrous **oxide** to form an **oxynitride layer** with uniform **nitrogen concentration** profile.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) a method of forming a MOS transistor comprising providing a substrate, forming a gate dielectric layer on the substrate, forming a conductive layer on the gate dielectric layer, forming sidewall structures adjacent to the conductive layer, and forming source and drain regions in the substrate adjacent to the sidewall structures; and
(b) a MOS transistor comprising a silicon substrate, a gate dielectric layer on the silicon substrate, a conductive layer, sidewall structures adjacent to the conductive layer, and source and drain regions in the silicon substrate adjacent to the sidewall structures.
USE - Forming MOS transistor gate dielectric layers.
ADVANTAGE - The process forms an asymmetric transistor without degradation in transistor performance. The reliability of the MOS transistor (i.e. its immunity to hot carrier degradation) is improved over that of pure silicon oxide since the uniform **nitrogen concentration** is above 6 atomic%. The layers formed have no **measurable** hydrogen.
DESCRIPTION OF DRAWING(S) - The figure shows a plot involved in the formation of metal oxide semiconductor transistor gate dielectric layer.
Dwg.3c/4
TECH US 2002072177 A1UPTX: 20021026
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The exposure of **oxide layer** to the high density nitrogen plasma is carried out at 700-900 watts. The annealing step is carried out by rapid thermal annealing at 800-1100 degrees C for 10-60 seconds.
Preferred Dimensions: The dielectric **layer** has a **thickness** of less than 40 Angstrom.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred **Concentration** : The uniform **nitrogen concentration** is greater than 6 atomic% and it describes a **nitrogen concentration** with less than 10% variation across the gate dielectric layer.
FS CPI EPI
FA AB; GI
MC CPI

L147 ANSWER 42 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1972:132473 HCAPLUS
DN 76:132473
TI Kinetics of thermal growth of **ultrathin** layers of silicon dioxide on silicon. I. Experiment
AU Van der Meulen, Y. J.
CS Thomas J. Watson Res. Cent., IBM, Yorktown Heights, NY, USA
SO Journal of the Electrochemical Society (1972), 119(4), 530-4
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
CC 70 (Crystallization and Crystal Structure)
AB The rate of formation of very thin SiO2 films thermally grown on [111] and [100] oriented Si wafers was studied by using ellipsometry to **measure** oxide **thickness**. **Film thicknesses** from 10 to 300 .ANG. were obtained by varying the oxidn. time, oxidn. temp. (700-1000.degree.), and O **concn**. in O-**N** mixts. at 1 atm total pressure. The applicability of ellipsometry for such a study is discussed. Reproducibility of **oxide films** grown to **thicknesses** of 20-30 .ANG. was .apprx..+-.1.0 .ANG.. Under otherwise equal conditions the oxide **thickness** differs for [100] and [111] oriented wafers. The pressure and temp. dependence of the linear rate const., klin, show that the SiO2 growth reaction is more complicated than was suggested earlier. In particular, a different pressure dependence for the 2 substrate orientations used indicates that several O species participate in the rate-detg. steps.
ST growth silicon dioxide layer; silicon substrate silicon dioxide
IT Ellipsometry
(of silica films)

L147 ANSWER 14 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1986-169531 [26] WPIX
DNN N1986-126483 DNC C1986-072831
TI IC device with **nitrided** silicon di oxide layer - having specific **nitrogen** content profile.
AW INTEGRATE CIRCUIT.
DC L03 U11 U12
IN CHANG, C C; KAHNG, D; KAMGAR, A; PARRILLO, L C
PA (AMTT) AMERICAN TELEPHONE & TELEGRAPH CO
CYC 15
PI WO 8603621 A 19860619 (198626)* EN 18p
RW: AT BE CH DE FR GB IT LU NL SE
W: JP KR
US 4623912 A 19861118 (198649)
EP 205613 A 19861230 (198652) EN
R: BE DE FR GB IT NL SE
JP 62501184 W 19870507 (198724)
ES 8801968 A 19880516 (198826)
CA 1260364 A 19890926 (198944)
EP 205613 B 19900711 (199028)
R: BE DE FR GB IT NL SE
DE 3578656 G 19900816 (199034)
KR 9600378 B1 19960105 (199905) H01L021-314
ADT WO 8603621 A WO 1985-US2243 19851113; US 4623912 A US 1984-678569 19841205; EP 205613 A EP 1985-901000 19851113; JP 62501184 W JP 1985-501072 19851113; ES 8801968 A ES 1985-549560 19851204; KR 9600378 B1 WO 1985-US2243 19851113, KR 1986-700526 19860805
PRAI **US 1984-678569 19841205**
REP 4.Jnl.Ref; EP 6706
IC C30B031-06; **H01L021-31**; H01L029-34
ICM H01L021-314
ICS C30B031-06; **H01L021-31**; H01L029-34
AB WO 8603621 A UPAB: 19990302
IC device has a **nitrided** SiO2 layer in which the at concn. fraction at the top surface is above 0.13, falling to below this **value** at a depth of about 30 Angstrom or less and to a **value** below 0.05 at a second depth about twice the first. The layer **thickness** is pref. 50-400 Angstroms.
USE/ADVANTAGE - An MOS transistors, capacitors etc. Layer may be formed by very rapid **nitriding** to avoid impurity diffusion, junction shifting etc. in the underlying active areas.
Dwg.5/5
ABEQ EP 205613 B UPAB: 19930922
1. A **process** of manufacturing an integrated cicruit including the step of **nitriding** a silicon dioxide layer to form a **nitrided** silicon dioxide layer having a top surface and a bottom surface, the bottom surface being physical contact with an underlying monocrystalline silicon semiconductor medium, characterized by the step of rapid thermal annealing a silicon dioxide layer to a temperature of at least about 1200 degrees C for a time interval equal to less than about two minutes while a major surface of the silicon dioxide layer is exposed to an ambient containing **nitrogen**, whereby the silicon dioxide layer is **nitrided**, and whereby the **nitrogen** fraction in the **nitrided** silicon dioxide layer falls from a **value** above about 0.13 at the top surface to a **value** below about 0.13 at a first distance of about 3nm or less from said top surfaces and further falls to a **value** below about 0.05 at a second dis-tance of about 6 nm or less from said top durface.
ADVANTAGE - Reduces size of microswitch as well as its wt. and simplifies mfr.
9).
ABEQ US 4623912 A UPAB: 19930922
**Nitrided** Si dioxide layer has a **N** fraction at the top surface greater than 0.13. The **N** fraction in the layer falls to below 0.13 at a first distance of 30 Angstroms or less from the surface an

to below 0.05 at a distance of twice the first distance or less from the surface.

A semiconductor integrated circuit is also claimed comprising the above **nitrided** Si dioxide layer, esp. a MOS transistor on which a **nitrided** dioxide layer **gate** dielectric is provided.

USE/ADVANTAGE - VLSI circuits mfr. in which undesirable charge trapping phenomena are avoided.

5/5

FS CPI EPI

FA AB

L13 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1989:106075 HCAPLUS
DN 110:106075
TI Electrical and physical properties of ultrathin **reoxidized** nitrided oxides prepared by rapid thermal processing
AU Hori, Takashi; Iwasaki, Hiroshi; Tsuji, Kazuhiko
CS Semicond. Res. Cent., Matsushita Electr. Ind. Co., Ltd., Moriguchi, 570, Japan
SO IEEE Transactions on Electron Devices (1989), 36(2), 340-50
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 67
AB Rapid thermal processing is applied to the full fabrication process of ultrathin **reoxidized** nitrided oxides (of gate dielecs.) for the first time. The 7.7-nm-thick oxides nitrided at various conditions were **reoxidized** at 900-1150.degree. for 15-600 s. As **reoxidn**. proceeds, the initial fixed charge d. shows a tunaround for a given temp.: at first it increases, reaches a max., and then decreases gradually. Nitridation- and **reoxidn**.-condition dependences of charge-trapping properties, i.e., the flat-band voltage shift (.DELTA. VFB) and the increase of midgap interface state d. (.DELTA.Ditm) induced by a high-field stress, where studied. Both the .DELTA.VFB and .DELTA.Ditm decrease monotonically as **reoxidn**. proceeds except for extraordinary heavy **reoxidns**. Both decrease more rapidly as the **reoxidn**. temp. is raised. The H **concn**. in the film [H] and the N **concn**. near the Si-SiO2 interface [N]int were extensively measured by SIMS and Auger electron spectroscopy, resp. As **reoxidn**. proceeds, the [H] decreases monotonically, while the [N]int changes little. The .DELTA.VFB decreases with the redn. of [H] following a proportional relation regardless of the [N]int. In contrast, the behavior of .DELTA.Ditm is explained readily by a 2-factor model: one factor is [H], which increases .DELTA.Ditm, and the other is [N]int, which reduces it. We derive the following semi-empirical formula: .DELTA.Ditm .varies. [H]2.5/(1 + KN . [N]2int), where KN is a const. Thus, the striking improvement of the charge-trapping properties by rapid **reoxidn**. is achieved by the redn. of [H] while keeping [N]int unchanged. If **reoxidn**. is extraordinarily heavy (e.g., at 1150.degree. for 200 s), however, both the .DELTA.Ditm and the abs. value of .DELTA. VFB increase again.

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1990:642446 HCAPLUS
DN 113:242446
TI Inversion layer mobility under high normal field in nitrided-oxide MOSFET's
AU Hori, Takashi
CS Semicond. Res. Cent., Matsushita Electr. Ind. Co., Ltd., Moriguchi, 570, Japan
SO IEEE Transactions on Electron Devices (1990), 37(9), 2058-69
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB The inversion layer mobility μeff under effective normal field Eeff higher than 0.5 MV/cm at 298 and 82 K are studied for the first time in MOSFET's with nanometer-range thin (reoxidized) nitrided oxides prepd. by rapid thermal processing (RTP) at 900-1150°C for 15-300 s. At an operating temp. of 298 K, while μeff of a pure oxide is degraded much faster than proportionally to Eeff-1/3 when Eeff > ~0.5 MV/cm, a nitrided oxide keeps a relationship μeff ∞ Eeff-1/3 up to Eeff of 1.1 MV/cm. Also at 82 K, μeff for a nitrided oxide is degraded much more slowly than that of an oxide having the -2 power Eeff dependence. As nitridation proceeds, while peak μeff degrades slowly, remarkable improvement of field-effect mobility μFE under high Eeff takes place very rapidly and then sats. As a result, μeff under high Eeff shows a turnaround with progress of nitridation: it increases at first, reaches a max. at a low AES-measured nitridation concn. of 2-3 at %, and then decreases gradually to a value lower than the oxide's μeff. Thus a light nitridation is favorable from the performance improvement point of view; e.g., the μeff at Eeff = 1 MV/ cm for a typical nitrided oxide is much larger by 30 (50) % than that of a pure oxide at 298 (82) K. Nitridation also avoids neg. gm obsd. at 82 K for an oxide MOSFET. These improvements remain substantially unchanged by addnl. reoxidn. and inert annealing. Contrary to the n-channel case described above, degradiations in mobility and gm with increasing Eeff and VG-VT for p-channel FET's are enhanced by nitridation, which is recovered to some extent by the subsequent reoxidn. A model of interface states located inside the bands is proposed to explain the contrasting effects of nitridation on high-field and hole mobilities.

L147 ANSWER 37 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1989:122008 HCAPLUS
DN 110:122008
TI Compositional study of **ultrathin** rapidly reoxidized nitrided oxides
AU Hori, Takashi; Iwasaki, Hiroshi; Ohmura, Takuichi; Samizo, Atsuko; Sato, Minoru; Yoshioka, Yoshiaki
CS Basic Res. Lab., Matsushita Electr. Ind. Co., Ltd., Moriguchi, 570, Japan
SO Journal of Applied Physics (1989), 65(2), 629-35
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
CC 66-3 (Surface Chemistry and Colloids)
Section cross-reference(s): 76, 79
AB **Ultrathin** nitrided oxides (7.7 nm) were reoxidized for the first time by lamp-heated rapid thermal annealing in O2 at 900-1150.degree. for 15-600 s. Compns. and residual H contents in various reoxidized nitrided oxides were studied by Auger electron spectroscopy (AES) and SIMS, resp. The AES analyses show that as reoxidn. proceeds, the **N concn.** peak near the outer surface decreases rapidly, while that near the Si-SiO2 interface [N]int decreases very slowly. A novel finding is that the N-rich layer near the Si-SiO2 interface moves further into the substrate as reoxidn. proceeds, following a movement similar to that of the Si-SiO2 interface. As the starting N content is lowered or the reoxidn. temp. is raised, the distance of the peak movement **.DELTA** .dAES and the redn. of [N]int are larger. The **.DELTA.**dAES is in quant. good agreement with the increase of **film thickness** evaluated by capacitance-voltage **measurements**. The movements are due to the diffusion-limited interfacial oxidn. In contrast to reoxidn., annealing in N2 of nitrided oxides scarcely reduces the [N]int and does not increase **.DELTA.**dAES. The SIMS analyses show that as reoxidn. proceeds, H concn. [H] in the film decreases monotonically. As the starting N content is lowered or the reoxidn. temp. is raised, [H] decreases more rapidly. Electron trapping was **monitored** by flat-band voltage shift **.DELTA.**VFB under high-field stress, and **.DELTA.**VFB decreased with the redn. of [H] following a proportional relation regardless of the fabrication condition. The [H] is also reduced by annealing in N2 and the redn. is **comparable** to that by reoxidn.
ST oxidn nitridation silicon surface; nitride oxide silicon surface compn; reoxidn nitrided oxide silicon surface; hydrogen nitrided oxide silicon surface

L147 ANSWER 13 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1991-135656 [19] WPIX
DNN N1992-105838 DNC C1992-065745
TI ONO inter-poly-composite dielectric for EPROM - has second **oxide layer** thick enough to prevent long-term charge loss from poly silicon electrode or nitride layer under high positive potential.
AW OXIDE-NITRIDE-OXIDE SANDWICH.
DC L03 U11 U12 U13 U14
IN CHENGSHENG, P; FREIBERGER, P E; LEOPOLDO, DY; SERY, GE
PA (ITLC) INTEL CORP
CYC 2
PI JP 03071674 A 19910327 (199119)*
US 5104819 A 19920414 (199218)B 13p
ADT JP 03071674 A JP 1990-184439 19900713; US 5104819 A US 1989-390158 19890807
PRAI US 1989-390158 19890807
IC H01L021-26; H01L029-78
AB JP 03071674 A UPAB: 20030317
**Method** comprises (A) coating on a surface of a semiconductor element a soln. in diglyme (solvent) of modified polyimide resin obtd. by addn. or condensn. reaction of a cpd. having at least one gp. selected from acryloyl gp., methacryloyl gp. and acetylenyl gp. with a polyimide resin which contains: (1) acid anhydride having the formula (I); (2) aromatic diamine having the formula (II) where Ar = trivalent aromatic gp., and R1 = -OH, -COOH or -SH gp., and (3) organopolysiloxane having the formula (III) where R2 = 1-12C divalent aliphatic hydrocarbon gp. or 6-10C aromatic hydrocarbon gp.; R3-6 = 1-12C aliphatic hydrocarbon gp. or 6-10C aromatic hydrocarbon gp.; **n** = 5-50, **amts.** of cpd. (3) = 5-60wt.% of the amts. of cpds. (1), (2) plus (3).
(B) curing the coated layer by irradiation of UV or electrons and then, (C) developing the coating layer to form a pattern.
USE/ADVANTAGE - Photosensitive polyimide acts as a buffer coat. High reliability and high heat resistance. @(8pp Dwg.No.0/0)@
ABEQ US 5104819 A UPAB: 19930928
An EPROM **process**, which includes fabricating a capacitor dielectric over a poly-Si electrode to inhibit long- term charge loss, comprises forming a silica layer (38) over a poly-Si electrode (35), forming a Si3N4 layer (39) over and thicker than the silica layer, followed by a second silica layer (40), thicker than the first and at least as thick as the nitride, and forming a control **gate** (42). The second silica layer is thick enough to prevent charge loss from either the first poly-Si electrode or the nitride layer when a high positive potential is applied to the control electrode.
Further claimed is a **process** in which the second **oxide layer** is chemically deposited over the nitride, forms at least part of the **gate** dielectric of peripheral transistors comprising 50-100 Angstrom of oxide deposited over 10- 100 Angstrom of thermal oxide Additionally claimed is an EPROM **process** in which the second **oxide layer** is at least 50 Angstrom thick and the composite dielectric (37) has a capacitively **measured** effective **thickness** of 200 Angstrom or less. Also claimed is a **process** e in which the composite dielectric **thickness** as **measured** above is 250 Angstrom or less and the nitride layer is 150 Angstrom or less.
USE/ADVANTAGE - **Processes** using ONO interpoly dielectrics for inhibiting long-term charge loss in EPROM cells (claimed) are provided. reliable composite dielectrics are formed in high yield and prior problems of **layer thickness, oxide** defects and low breakdown voltages are overcome. (First major country equivalent to J03071674-A)
FS CPI EPI
FA AB; GI
MC EPI: U11-C05B9; U12-D02A1; U14-A03B7; U11-C18B5; U13-C04A

L147 ANSWER 35 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1994:13359 HCAPLUS
DN 120:13359
TI Growth of **oxide layers** on thin aluminum nitride **samples measured** by electron energy-loss spectroscopy
AU Sternitzke, Martin
CS Dep. Mater. Sci., Univ. Darmstadt, Darmstadt, D-64287, Germany
SO Journal of the American Ceramic Society (1993), 76(9), 2289-94
CODEN: JACTAW; ISSN: 0002-7820
DT Journal
LA English
CC 57-2 (Ceramics)
AB AlN ceramics with different amts. of oxygen impurities were investigated by EELS. Because of the high dynamics of EEL spectra, a method was developed to record partial spectra and then to join them together to form a complete spectrum. The data obtained from EEL spectra were the **nitrogen**/oxygen **concn.** ratio, **sample thickness**, and energy-loss near-edge structures (ELNES). Because of spontaneous formation of an **oxide layer** on AlN **samples** immediately after ion milling, a method had to be developed which yielded the **oxide layer thickness** and the bulk oxygen content. The growth kinetics of the **oxide layer** were investigated by exposing the AlN **samples** at room temp. to air and to water for various times. From these **measurements** a logarithmic rate law for the oxidn. of AlN at room temp. was obtained.
ST aluminum nitride ion milling oxide growth
IT Ceramic materials and wares
(aluminum nitride, ion milling of, oxide growth in, EELS study of)
IT 24304-00-5, Aluminum nitride

L147 ANSWER 34 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1995:687572 HCAPLUS
DN 123:274551
TI Ion beam analysis of **ultrathin** dielectric films
AU Baumvol, I. J. R.; Rolfs, C.
CS Instituto de Fisica - UFRGS, Porto Alegre - RS, 91501-970, Brazil
SO Nuclear Instruments & Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms (1995), 99(1-4), 431-5
CODEN: NIMBEU; ISSN: 0168-583X
PB Elsevier
DT Journal
LA English
CC 79-6 (Inorganic Analytical Chemistry)
Section cross-reference(s): 76
AB Nuclear reaction anal. and nuclear resonance profiling methods are currently used to study Si-based **ultrathin** (**thickness** <10 nm) dielec. **films**, like Si **oxide**, Si nitride and Si oxynitrides. The nuclear reactions were used to **measure** the total **amts**. of H, **N** and O isotopes that take part in the films, with sensitivities .gtoreq.1012 atoms cm-2. Nuclear resonance profiling and also step-by-step chem. etching assocd. with nuclear reaction analyses were used to **measure** the concn. vs. depth profiles of H, N, O and Si isotopes with depth resolns. of .apprx.1 nm. Also, channeling of alpha-particles combined with detection at very grazing angles was used to **measure** the av. stoichiometry of the **ultrathin** films.
ST ion beam analysis **ultrathin** dielec film

4/9/14
DIALOG(R)File 2:INSPEC


5334553 INSPEC Abstract Number: B9609-2570D-003
Title: Recent developments in N/sub 2/O/NO-based ultra thin oxynitride **gate** dielectrics for CMOS ULSI applications
Author(s): Han, L.K.; Bhat, M.; Wristers, D.; Wang, H.H.; Kwong, D.L.
Author Affiliation: Dept. of Electr. & Comput. Eng., Texas Univ., Austin, TX, USA
Conference Title: 1995 4th International Conference on Solid-State and Integrated Circuit Technology. Proceedings (Cat. No.95TH8143) p.80-4
Editor(s): Baldwin, G.L.; Li, Z.; Tsai, C.C.; Zhang, J.
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 798 pp.
ISBN: 0 7803 3062 5 Material Identity Number: XX95-02106
Conference Title: Proceedings of 4th International Conference on Solid-State and IC Technology
Conference Sponsor: Chinese Inst. Electron.; IEEE Electron Devices Soc
Conference Date: 24-28 Oct. 1995 Conference Location: Beijing, China
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); General, Review (G)
Abstract: This paper reviews recent developments in N/sub 2/O- and NO-based oxynitride **gate** dielectrics for CMOS ULSI applications. These dielectrics are extremely attractive due to their process simplicity, thickness controllability, and excellent electrical characteristics. In this paper, several issues like thickness scaling, growth kinetics, chemical composition, electrical properties, hot-carrier reliability, and EEPROM applications of these dielectrics are discussed. (29 Refs)
Subfile: B
Descriptors: CMOS memory circuits; dielectric thin films; EPROM; hot carriers; integrated circuit reliability; MOSFET; nitridation; silicon compounds; **thickness control**; ULSI
Chemical Indexing:
Si-SiON int - SiON int - Si int - **N** int - **O** int - SiON ss - Si ss - **N** ss - **O** ss - Si el (Elements - 1,3,3)
N2O bin - N2 bin - **N** bin - **O** bin (Elements - 2)
NO bin - **N** bin - **O** bin (Elements - 2)

L13 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:57770 HCAPLUS
DN 124:190559
TI Monolayer nitrogen-atom distributions in ultrathin gate dielectrics by low-temperature low-thermal-budget processing
AU Lucovsky, Gerald; Lee, David R.; Hattangady, Sunil V.; Niimi, Hiro; Jing, Ze; Parker, Chris; Hauser, John R.
CS Department of Physics, North Carolina State University, Raleigh, NC, 27695-8202, USA
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1995), 34(12B), 6827-37
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 66, 78
AB The research reported in this paper is based on an approach to low-temp./low-thermal budget device fabrication that combines plasma and rapid thermal processing, and which was customized to control sep. (i) the N-atom bonding chem. and compn. profiles, and (ii) the structural and chem. relaxations in stacked gate structures. Control of N-atom incorporation at the monolayer level at the cryst.- and polycryst.-Si interfaces, and at alloy levels within the bulk dielecs. was achieved by combining low-temp. (.apprx.300.degree.) plasma-assisted processes to generate the N-atom **concn**. profiles, with low-thermal-budget rapid thermal annealing (RTA) to promote chem. and structural relaxations that minimize defects and defect precursors. Device measurements indicate that N-atom incorporation improves reliability with respect to hot carrier degrdn. of field effect transistors.

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1996:210711 HCAPLUS
DN 124:303695
TI Degradation of oxynitride gate dielectric reliability due to boron diffusion
AU Wristers, D.; Han, L. K.; Chen, T.; Wang, H. H.; Kwong, D. L.; Allen, M.; Fulford, J.
CS Microelectronic Research Center, University of Texas, Austin, TX, 78712, USA
SO Applied Physics Letters (1996), 68(15), 2094-6
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB The authors report on the impact of the suppression of B diffusion via nitridation of SiO2 on gate oxide integrity and device reliability. SiO2 subjected to rapid thermal nitridation in pure nitric oxide (NO) was used to fabricate thin oxynitride gate dielecs. Both n+ polycryst. Si (polysilicon) gated n-MOS (metal-oxide semiconductor) and p+-polysilicon gated p-MOS devices were subjected to anneals of different times to study the effect of dopant diffusion on gate oxide integrity. As expected, an advanced oxynitride gate dielec. will effectively alleviate the B-penetration-induced flat band voltage instability in p+-Si gated p-MOS capacitors due to the superior diffusion barrier properties. However, such improvements are obsd. in conjunction with some degrdn. of the oxide reliability due to the B-blocking/accumulation inside the gate dielec. Even though the oxide quality is slightly degraded for NO-nitride SiO2 with p+-polysilicon gates, p-MOSFETs (metal-oxide semiconductor field effect transistors) with these dielecs. still show improved interface stability compared to conventional SiO2 due to the reduced B penetration into the Si/SiO2 interface and underlying channel region.

L147 ANSWER 32 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:250377 HCAPLUS
DN 124:329415
TI Dry oxidation mechanisms of thin dielectric films formed under N2O using isotopic tracing methods
AU Ganem, J.-J.; Rigo, S.; Trimaille, I.; Baumvol, I. J. R.; Stedile, F. C.
CS Groupe Phys. Solides, Univ. Paris 6 et 7, Paris, 75251, Fr.
SO Applied Physics Letters (1996), 68(17), 2366-8
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The authors investigated the mechanisms of thermal reoxidn. in dry O2 of silicon **oxynitride films** prepd. by processing Si(100) wafers in a rapid thermal furnace in a pure nitrous oxide (N2O) ambient, using isotopic tracing of oxygen and nitrogen. Std. nuclear reaction analyses for the **measurement** of the total amts. of the different isotopes, and very narrow resonant nuclear reactions for high resoln. (1 nm) depth profiling of these elements were used. The silicon **oxynitride films** grown in pure 15N216O were 8-nm thick, with a small **amt.** of **nitrogen** localized near the interfacial region. Under reoxidn. in dry 18O2, the **thickness** of the dielec. **film** increased while a pronounced isotopic exchange took place between the 18O from the gas and the 16O from the film, as well as a significant loss of 15N. This is in contrast with the reoxidn. in dry O2 of pure SiO2 films, where the oxygen exchange is rather small as **compared** to that obsd. in the present case.
ST silicon **oxynitride film** thermal reoxidn; nitrous oxide silicon oxide nitride formation

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1996:278912 HCAPLUS
DN 124:357639
TI Influence of nitrogen profile on electrical characteristics of furnace- or rapid thermally nitrided silicon dioxide films
AU Bouvet, D.; Clivaz, P. A.; Dutoit, M.; Coluzza, C.; Almeida, J.; Margaritondo, G.; Pio, F.
CS Inst. Micro- optoelectronics, Swiss Federal Inst. Technol., Lausanne, CH 1015, Switz.
SO Journal of Applied Physics (1996), 79(9), 7114-7122
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB Thin SiO2 films nitrided in N2O by rapid thermal processing (RTP) or in a classical furnace were studied by XPS, secondary ion mass spectroscopy, and elec. measurements on metal-oxide-semiconductor capacitors. Differences between the two nitridation processes were obsd. and explained. In lightly nitrided films, N occupies two configurations. N is bound to three Si atoms with at least one in the substrate or all three in the oxide. In RTP-nitrided films, both of these species are confined to within 1.5 nm of the Si/SiO2 interface. In furnace-nitrided films, the 1st species is also located close to the interface whereas the 2nd one fills most of the regrown oxide thickness. In furnace-grown films, which are more heavily nitrided, a 3rd structure due to Si2=N-O is obsd. throughout the layer. The elec. characteristics are well correlated with the amt. of N at the interface that is bound to Si atoms in the substrate.

L15 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:262769 HCAPLUS
DN 126:337243
TI Unified model of boron diffusion in thin gate oxides: effect of F, H2, N, oxide thickness, and injected Si interstitials
AU Fair, Richard B.
CS Dept. Electrical Computer Engineering, Duke University, Durham, NC, 27708, USA
SO Technical Digest - International Electron Devices Meeting (1995) 85-88
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The first unified network-defect-level model for B diffusion in SiO2 is described for use in process simulation. Models were developed to explain the Si processing effect on B diffusion through thin gate oxides. With these models the enhanced B diffusion effect in poly Si/SiO2 structures can be **predicted** from BF2 implants, wet oxidn., and exposure to H2 ambients, and the concn. of N in nitrided oxides in reducing B diffusion. It has been shown for the first time that there is an oxide thickness dependence on B diffusion.
IT 1333-74-0, Hydrogen, uses **7727-37-9**, Nitrogen, uses 7782-41-4, Fluorine, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(effect of F, H2, N, **oxide** thickness, and injected Si interstitials on boron diffusion in thin **gate oxides**
)

L147 ANSWER 31 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:548508 HCAPLUS
DN 127:270951
TI Physical and electrical properties in metal-oxide-silicon capacitors with various **gate** electrodes and **gate** oxides
AU Chang-Liao, K.-S.; Chen, L.-C.
CS Department of Nuclear Engineering and Engineering Physics, National Tsing Hua University, Hsinchu, Taichung, Taiwan
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (1997), 15(4), 942-947
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The phys. and elec. properties of metal-oxide-silicon (MOS) capacitors with the **gate** electrodes deposited using poly-Si or amorphous-Si (a-Si) and with the **gate** oxide grown in O2 or N2O have been investigated. The differences of a **gate** oxide grown in N2O with a conventional furnace and an **oxide film** annealed in N2O by a rapid thermal **process** (RTP) were also studied. Anal. of phys. properties included the **thickness** variations of **oxide films**, the shrink ratios of **gate** electrode films, the **nitrogen** and hydrogen **concns**. in oxides, and SiO2/Si interfacial strain. The **measurement** of elec. properties in MOS capacitors included the interface trap d. (Dit), the charge-to-breakdown, and the hot electron and radiation induced Dit and flatband voltage shifts. To improve the elec. reliability of MOS devices with **ultrathin gate** oxides, an oxynitride should be introduced although some properties of it are slightly inferior to those of conventional oxides. The combination of a **gate** electrode deposited using a-Si and a **gate** oxide annealed in N2O using RTP is shown to exhibit excellent charge-to-breakdown performance and to reduce hot electron and radiation induced interface traps. This improvement can be explained using a mechanism based on the release of compressive stress in the oxide and the relaxation of SiO2/Si interfacial strain, which could be qual. analyzed using IR spectra.
ST silicon MOS capacitor **gate** electrode oxide

L147 ANSWER 30 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:185889 HCAPLUS
DN 129:47814
TI Elastic recoil detection using time-of-flight for analysis of TiN/AlSiCu/TiN/Ti contact metalization structures
AU Gujrathi, S. C.; Gagnon, G.; Fortin, V.; Caron, M.; Currie, J. F.; Ouellet, L.; Tremblay, Y.
CS Groupe des Couches Minces (GCM), Department of Physics, Station Centre-Ville, Universite de Montreal, Montreal, QC, H3C 3J7, Can.
SO Nuclear Instruments & Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms (1998), 136-138, 661-668
CODEN: NIMBEU; ISSN: 0168-583X
PB Elsevier Science B.V.
DT Journal
LA English
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 56, 57
AB The ability of elastic recoil detection (ERD) with time-of-flight (TOF) to quantify multilayer TiN/AlSiCu/TiN/Ti contact metalization structures on Si and SiO2 has been demonstrated. In the technique a single microchannel plate (MCP) detector assembly and a silicon surface barrier detector (SSBD) were used. Tech. high quality multilayer structures that have important applications in VLSI/ULSI devices were produced in a com. Varian M2000 cluster tool by sputtering techniques. Several device process parameters such as annealing temp. (450.degree.C, 500.degree.C and 550.degree.C), TiN **oxidn.**, TiN ARC **layer**, TiN diffusion barrier **thickness** (50 and 90 nm) and types of substrate (Si and SiO2) have important consequences on the performance of the product. The effect of **changes** in the above mentioned parameters on the elemental compn. have been reliably studied by ERD. All the elements from H to Cu including substrate Si of a contact structure have been quant. and simultaneously profiled in a single expt. The reproducibility of the major **concns.** (**N**, O, Al, Si and Ti) in a multilayer test **sample** in every batch was within .+-.5%. Grazing angle X-ray diffraction (XRD) and the analyses of the ternary and quaternary phase diagrams complemented by the ERD investigations have been used to identify various phases in the layers. These results were then correlated with the **measured** elec. properties.
ST titanium nitride diffusion barrier contact metalization; elastic recoil detection contact metalization structure

L30 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:563069 HCAPLUS
DN 129:284104
TI Isotopic labeling studies of oxynitridation in nitric oxide (NO) of Si and SiO2
AU Trimaille, I.; Ganem, J.-J.; Gosset, L. G.; Rigo, S.; Baumvol, I. J. R.; Stedile, F. C.; Rochet, F.; Dufour, G.; Jolly, F.
CS Groupe de Physique des Solides, Universite Paris 7, Universite Paris 6, UMR 75-88 CNRS, PARIS, 75251, Fr.
SO NATO Science Series, 3: High Technology (1998), 47(Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices), 165-179
CODEN: NSSTFF
PB Kluwer Academic Publishers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB Rapid thermal oxynitridation in nitric oxide (NO) of a thick (14 nm) SiO2 film grown on Si(001) is studied as a first stage towards understanding of at. transport mechanisms occurring during NO annealing of thin SiO2 films. The SiO2 films were grown in an ultra high vacuum rapid thermal processing (RTP) furnace in static pressure of natural O2 (16O2). These films were then annealed in 15N and 18O-enriched NO (15N18O) for 20 and 80 s. Total amts. of nitrogen and oxygen and heavy isotopes depth distribution were measured using non resonant and resonant nuclear reactions anal. The results are discussed in terms of at. depth profiles and growth mechanisms. These first results are more likely explained by two mechanisms occurring in parallel. In the first one, NO diffuses through the silica network without reacting with it and both N and O are fixed in the near interface region. In the second one, 18O is fixed near the oxide surface due to a mechanism related with a step-by-step motion of network oxygen atoms, by a simple diffusion process, induced by the presence of network defects, involving O only. This latter mechanism leads mostly to an exchange of oxygen atoms between the oxide network and the gas phase. Direct oxynitridation of Si(001) in nitric oxide (NO) is studied as a **function** of gas pressure. The dielec. films were grown in the RTP furnace in static pressures of 15N and 18O-enriched NO (15N18O). The nuclear reactions techniques mentioned above were employed to analyze the dielec. films. The **thicknesses** of the oxynitrides formed in NO never exceeded 3 nm, in our thermal treatments conditions. At 1050 .degree.C, for isochronal thermal treatments, the amts. of nitrogen fixed in the films decreases as the pressure P of NO increases (in the range 1 to 100 hPa) suggesting that nitrogen atoms may be fixed via a vacancy mechanism. The amt. of nitrogen atoms was found to support a P-1/4 law, whereas in N2O the nitrogen amt. varies as P1/2. The areal densities of oxygen atoms are consistent with a P1/4 law, as in the case of N2O oxynitridation. Angle Resolved XPS (AR-XPS) for different incident angles was used as a complementary technique to provide informations on bonding structures and their distributions. AR-XPS results on the analyzed samples show no evidence of N-O bonds.

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1999:14882 HCAPLUS
DN 130:161164
TI Characterization of ultra-thin oxides using electrical C-V and I-V measurements
AU Hauser, J. R.; Ahmed, K.
CS Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, 27695, USA
SO AIP Conference Proceedings (1998), 449(Characterization and Metrology for ULSI Technology), 235-239
CODEN: APCPCS; ISSN: 0094-243X
PB American Institute of Physics
DT Journal
LA English
AB The measurement of elec. parameters from capacitance-voltage (C-V) and current-voltage (I-V) curves provides a fast means of characterizing oxides in MOS capacitors or transistor structures. For ultra-thin oxides (< 2 nm), conventional, well-established techniques must be reconsidered and modified due to several increasingly important phys. effects including polysilicon depletion and surface quantum mech. effects. In this work these effects have been incorporated into a rapid anal. program for extg. ultra-thin oxide parameters from measured C-V and I-V data. The technique uses a phys. based model of structure charge and potential combined with a non-linear least squares fitting technique to ext. device parameters.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1999:119352 HCAPLUS
DN 130:230511
TI Mechanism of low temperature nitridation of silicon oxide layers by nitrogen plasma generated by low energy electron impact
AU Mizokuro, Toshiko; Yoneda, Kenji; Todokoro, Yoshihiro; Kobayashi, Hikaru
CS The Institute of Scientific and Industrial Research, Osaka University, 8-1 Mihogaoka, Ibaraki, Osaka, 567-0047, Japan
SO Journal of Applied Physics (1999), 85(5), 2921-2928
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB Thermal silicon oxide layers formed on the Si substrate can be nitrided at low temps. ranging between 25 and 700° by nitrogen plasma generated by low energy electron impact. The nitrogen concn. is high near the oxide surface, and the nitrogen at. concn. ratio [N/(Si+O+N)] at the surface ranges between ~10% and ~25%, depending on the nitridation conditions. For nitridation >450°, only N≡Si3 (i.e., a nitrogen atom bound to three Si atoms) is obsd. in the nitrided oxide films by XPS measurements, while both N+:Si2 (i.e., an N+ ion bound to two Si atoms) and N≡Si3 are present with nitridation <400°. When a neg. bias voltage is applied to the Si with respect to the grid used for the generation of nitrogen plasma, the nitrogen concn. in the film increases, indicating that nitrogen cations play a dominant role in the nitridation. First, N+ ions react with SiO2 to form N+:Si2, after which inward movement of N+ ions occurs with the assistance of an elec. field induced in the nitrided oxide layers by nitrogen ions at the surface. Ultimately, N+:Si2 is transformed to N≡Si3.
RE.CNT 46 THERE ARE 46 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1999:263203 HCAPLUS
DN 130:359967
TI Plasma-assisted oxidation, anodization, and nitridation of silicon
AU Hess, D. W.
CS School of Chemical Engineering, Georgia Institute of Technology, Atlanta, GA, 30332, USA
SO IBM Journal of Research and Development (1999), 43(1/2), 127-145
CODEN: IBMJAE; ISSN: 0018-8646
PB International Business Machines Corp.
DT Journal
LA English
AB Plasma-assisted oxidn., anodization, and nitridation of silicon have been performed in microwave, radio-frequency, and d.c. plasmas with a variety of reactor configurations and a range of plasma densities. Compared to thermal processes at equiv. substrate temps., film growth rates are accelerated by the plasma-enhanced generation of reactive chem. species or by the presence of elec. fields to aid charged-particle transport during plasma processes. Oxidn., anodization, and nitridation kinetics, mechanisms, and film properties attainable with plasma enhancement are discussed for cryst., polycryst., and amorphous silicon layers and for silicon-germanium alloys. The use of these plasma methods for surface and interface modification of silicon-based materials and devices is described.
RE.CNT 103 THERE ARE 103 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L147 ANSWER 28 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:612236 HCAPLUS
DN 131:316279
TI Low damage nitridation of silicon oxide surfaces by remote-plasma-excited nitrogen
AU Saito, Yoji; Mori, Ukyo
CS Department of Electrical Eng. & Elec., Seikei University, Tokyo, 180-8633, Japan
SO Materials Research Society Symposium Proceedings (1999), 567(Ultrathin SiO2 and High-K Materials for ULSI Gate Dielectrics), 33-37
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB We incorporated significant d. of nitrogen only near the top surfaces of the thermally grown oxides by the fluorination at room temp. followed by **at. nitrogen** treatment around 550.degree.C. Av. **nitrogen concn.** of more than 6 percent was obtained in the nitrided **layer** with **thickness** below 1 nm. We fabricated MOS devices using the nitrided **oxide films** without hydrogenation, and **measured** capacitance-voltage characteristics. The d. of nitridation-induced interface defects in the MOS device was **estd.** to be below 2.times.1010cm-2. The proposed technique identifies a unique process for obtaining high quality **ultrathin** dielecs.
ST nitridation silicon oxide surface plasma excited nitrogen
IT MOS devices

ANSWER 1 HCAPLUS COPYRIGHT 2003 ACS on STN
Full Text
AN 1999:612376 HCAPLUS
DN 131:278620
TI Structure and bonding in nitrided oxide films by SIMS and XPS
AU Novak, S. W.; Shallenberger, J. R.; Cole, D. A.; Marino, J. W.
CS East Windsor, NJ, 08520, USA
SO Materials Research Society Symposium Proceedings (1999), 567(Ultrathin SiO2 and High-K Materials for ULSI Gate Dielectrics), 579-586
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB The N distribution and bonding in 5 types of oxynitride films were studied using SIMS and XPS. Films were grown using N2O, NO-O2, and NH3 gas sources, a remote plasma N source, and a Helicon plasma source. The SIMS measurements show different N distributions for each type of sample. XPS measurements show only N≡Si, bonding in the gas source films, N≡Si3 and O-N-Si2 bonding in the remote plasma sample, and N≡Si3, O-N≡Si2 and O2N-Si bonding in the Helicon plasma sample. Angle-resolved XPS measurements show that the O2N-Si bonding is deepest in the sample whereas the O-NSi2 bonding is assocd. with a surface oxide.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L30 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:651271 HCAPLUS
DN 131:315209
TI Characterization and production metrology of thin transistor gate oxide films
AU Diebold, Alain C.; Venables, David; Chabal, Yves; Muller, David; Weldon, Marcus; Garfunkel, Eric
CS SEMATECH, Inc., Austin, TX, 78741, USA
SO Materials Science in Semiconductor Processing (1999), 2(2), 103-147
CODEN: MSSPFQ; ISSN: 1369-8001
PB Elsevier Science Ltd.
DT Journal; General Review
LA English
CC 73-0 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
AB The **thickness** of SiO2 that was used as the transistor gate dielec. in most advanced memory and logic applications has decreased <7 nm. Unfortunately, the accuracy and reproducibility of metrol. used to measure gate dielec. **thickness** during manuf. of integrated circuits remains in some dispute. Detailed materials characterization studies resulted in a variety of descriptions for the oxide-interface-substrate system. Part of the problem is that each method measures a different quantity. Another related issue concerns how one should define and model the crit. dielec./substrate interface. As scaling continues, the interface between SiO2 and Si becomes a larger part of the total **thickness** of the oxide film. Although materials characterization studies have focused on this interface, there were few attempts to compare the results of these methods based on an understanding of the models used to interpret the data. In this review with 112 refs., the authors describe the phys. and elec. characterization of the interfacial layer. IR absorption data are reviewed and previous interpretations of the LO/TO phonon shifts as a **function** of oxide **thickness** are refined. The authors correlate the available results between phys. methods and between phys. and elec. methods. This information is essential to inclusion of an interfacial layer in optical models used to measure SiO2 inside the clean room. The authors also describe some characterization issues for nitride oxides.

L123 ANSWER 34 OF 34 JAPIO (C) 2003 JPO on STN
AN 2000-311928 JAPIO
TI JUDGMENT METHOD FOR **NITROGEN CONCENTRATION** IN GATE **OXIDE FILM**

2000 pub.

IN IWATA YASUSHI
PA SHARP CORP
PI JP 2000311928 A 20001107 Heisei
AI JP 1999-121090 (JP11121090 Heisei) 19990428
PRAI JP 1999-121090 19990428
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
IC ICM **H01L021-66**
ICS H01L029-78
AB PROBLEM TO BE SOLVED: To **estimate nitrogen concentration** on the basis of a simply **calculated** reoxidated **film thickness** rate by a method wherein the **nitrogen concentration** is judged on the basis of the deposition speed of a thermal **oxide film**.
SOLUTION: A thermal **oxide film** 2 is formed on a semiconductor substrate 1 by a CVD method. After that, the thermal **oxide film** 2 is heated for a short time in a nitrous oxide atmosphere, and an **oxynitride film** 3 is formed. After that, when the **oxynitride film** is heated for a short time in an oxygen atmosphere, the **oxynitride film** is reoxigized, and a reoxidation **film** 4 is formed. A reoxidation **film thickness** rate is found on the basis of a **film thickness** L1 after the **oxynitride film** is formed by oxidizing N2O and on the basis of a **film thickness** L2 after a reoxidation treatment performed thereafter. A thermal **oxide film thickness** which is found by an optical **film-thickness measuring** device is 40 Å as a target **film thickness**. A linear relationship is established between the **concentration** of **nitrogen** in a gate **oxide film** and a reoxidation rate. When the reoxidation rate with reference to the **oxynitride film** by a treatment under an oxynitriding condition is **calculated**, the **concentration** of the **nitrogen** can be **estimated**. By using this characteristic, the **concentration** of the **nitrogen** in the gate **oxide film** is judged.

L147 ANSWER 27 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:325523 HCAPLUS
DN 133:113344
TI High quality of **ultra-thin** silicon **oxynitride** **films** formed by low-energy nitrogen implantation into silicon with additional plasma or thermal oxidation
AU Diniz, J. A.; Sotero, A. P.; Lujan, G. S.; Tatsch, P. J.; Swart, J. W.
CS CCS and DSIF/FEEC, Universidade Estadual de Campinas, Campinas, Brazil
SO Nuclear Instruments & Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms (2000), 166-167, 64-69
CODEN: NIMBEU; ISSN: 0168-583X
PB Elsevier Science B.V.
DT Journal
LA English
CC 76-10 (Electric Phenomena)
AB Silicon oxynitride (SiOxNy) insulators have been obtained by low-energy mol. nitrogen ion (N2+) implantation in Si substrates prior to thermal or high d. O2 ECR (electron cyclotron resonance) or N2O RP (remote plasma) plasma oxidn. at temps. of 20 and 350.degree., resp. Characterization by Fourier transform IR (FTIR) analyses reveals the high structural quality and very low Si-**N** bond **concn**. of **oxynitride** **films**. The **film thicknesses** between 2.5 and 12 nm were found by ellipsometry using a fixed refractive index of 1.46. MOS capacitors, with Al electrodes and final sintering time at 420.degree. for 20-30 min in forming gas, were fabricated. A relative dielec. const. of 3.9 was adopted to ext. the effective charge densities from capacitance-voltage (C-V) curves, resulting in values between 4 .times. 1010 and 6 .times. 1011 cm-2. Breakdown elec. fields from 9-26 MV/cm were obtained from current-voltage (I-V) **measurements**. These results indicate that the obtained SiOxNy films are suitable gate insulators for metal-oxide-semiconductor (MOS) devices.
ST silicon **oxynitride film** gate insulator

L29 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:414709 HCAPLUS
DN 133:143050
TI Reliability of ultrathin silicon dioxide under combined substrate hot-electron and constant voltage tunneling stress
AU Vogel, Eric M.; Suehle, John S.; Edelstein, Monica D.; Wang, Bin; Chen, Yuan; Bernstein, Joseph B.
CS Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD, 20899, USA
SO IEEE Transactions on Electron Devices (2000), 47(6), 1183-1191
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB An exptl. investigation of breakdown and defect generation under combined substrate hot-electron and tunneling elec. stress of silicon oxide ranging in **thickness** from 2.0 nm to 3.5 nm is reported. Using independent control of the gate current for a given substrate and gate bias, the time-to-breakdown of ultrathin silicon dioxide under substrate hot-electron stress is obsd. to be inversely proportional to the gate c.d. The **thickness** dependence (2.0 nm to 3.5 nm) of substrate hot-electron reliability is reported and shown to be similar to const. voltage tunneling stress. The build-up of defects measured using stress-induced-leakage-current and charge-pumping for both tunneling and substrate hot-electron stress is reported. Based on these and previous results, a model is proposed to explain the time-to-breakdown behavior of ultrathin oxide under simultaneous tunneling and substrate hot-electron stress. The results and model provide a coherent understanding for describing the reliability of ultrathin SiO2 under combined substrate hot-electron injection and const. voltage tunneling stress.

L14 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:490035 HCAPLUS
DN 133:259898
TI Independent interface and bulk film contributions to reduction of tunneling currents in stacked oxide/nitride gate dielectrics with monolayer nitrided interfaces
AU Lucovsky, G.; Niimi, H.; Wu, Y.; Yang, H.
CS Campus Box 8202, Department of Physics, North Carolina State University, Raleigh, NC, 27695-8202, USA
SO Applied Surface Science (2000), 159-160, 50-61
CODEN: ASUSEE; ISSN: 0169-4332
PB Elsevier Science B.V.
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
AB Direct tunneling limits aggressive scaling of thermally-grown oxides to about .apprx.1.6 nm, a **thickness** at which the tunneling current at 1 V is .apprx.1 A/cm2. Exptl. results are supported by interface characterizations and model **calcns.**, which demonstrate that multi-layer or stacked gate dielecs. prepd. by remote plasma processing comprised of (i) ultra-thin nitrided SiO2 interface layers, and (II) either Si nitride or oxynitride bulk dielec. films, can extend the oxide-equiv. **thickness**, tox-eq, limit down to .apprx.1.1-1.0 nm. A similar stacked gate dielec., which substitutes higher-k oxides such as Zr(Hf)O2-SiO2 silicate alloys or Ta2O5 for the nitrides or oxynitride alloys, is projected to further reduce tox-eq to .apprx.0.6-0.7 nm.

L147 ANSWER 26 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:785519 HCAPLUS
DN 134:64346
TI Theoretical and experimental investigation of **ultrathin** oxynitrides
AU Demkov, A. A.; Liu, R.
CS Semiconductor Product Sector, Motorola, Inc., Mesa, AZ, USA
SO Materials Research Society Symposium Proceedings (2000), 592(Structure and Electronic Properties of Ultrathin Dielectric Films on Silicon and Related Structures), 257-262
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 65, 66, 73
AB Microscopic properties of thin oxynitrides were investigated using a combination of the IR ATR and ab-initio electronic structure methods. We use a theor. structural model based on the Si-SiO2 interface with the oxide **thickness** of 0.8 nm. The interfacial region amts. to .apprxeq.0.4 nm (the total **thickness** of the O contg. **layer** is 1.2 nm). The quantum mol. dynamics simulations suggest that N accumulates at the interface. We have generated **samples** with the **N concns.** from 1.69 .times. 1014 cm-2 to 6.78 .times. 1014 cm-2. The structural anal. of N contg. cells indicates a significant improvement of the **oxide layer** and the strain redn. at the interface. We have performed a **calcn.** of the vibrational d. of states. A N-localized mode at 809 cm-1 was identified. The exptl. IR ATR data is in qual. agreement with the **calcn.** The valence band offset **calcns.** reveal a 0.3 eV increase of the offset due to N at the highest **N concn** . considered. The valence band offset increase comes mainly from the structural **change** in the **oxide layer.** The interfacial dipole contributes 0.12 eV to the increase, while the structural **change** in the **oxide layer** gives addnl. 0.2 eV.
ST silicon silica interface oxynitride IR spectra electronic structure

L147 ANSWER 10 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1996-499566 [50] WPIX
DNN N1996-421375 DNC C1996-156132
TI Multi-level structured insulator suitable for MOS **gate** insulator - having **thicker** 1st dielectric film of oxide semiconductor and thinner second dielectric film of (oxy)**nitride** of semiconductor, acting as diffusion barrier to impurity atoms from **gate** electrode.
DC L03 U11
IN HASEGAWA, E
PA (NIDE) NEC CORP
CYC 5
PI EP 742593 A2 19961113 (199650)* EN 23p H01L029-51 <--
R: DE GB
JP 08306687 A 19961122 (199706) 7p H01L021-318 <--
EP 742593 A3 19971105 (199814) H01L029-51 <--
US 5972800 A 19991026 (199952) H01L021-316
US 6037651 A 20000314 (200020) H01L023-58
KR 266519 B1 20000915 (200134) H01L029-78 <--
ADT EP 742593 A2 EP 1996-107377 19960509; JP 08306687 A JP 1995-136169 19950510; EP 742593 A3 EP 1996-107377 19960509; US 5972800 A Div ex US 1996-644166 19960510, US 1997-890312 19970709; US 6037651 A US 1996-644166 19960510; KR 266519 B1 KR 1996-16033 19960510
PRAI **JP 1995-136169 19950510**
REP No-SR.Pub; 5.Jnl.Ref; EP 617461; JP 01315141; US 5393683
IC ICM H01L021-316; **H01L021-318**; H01L023-58; **H01L029-51**; **H01L029-78**
ICS H01L021-336
AB EP 742593 A UPAB: 19970212
The semiconductor device comprises a semiconductor substrate with a multi-level structured insulator formed thereon, the insulator comprising a **thicker** first dielectric film made of an oxide of a semiconductor which is a constituent of the substrate; and a thinner second dielectric film formed thereon and made of a **nitride** or oxynitride of the semiconductor which is a constituent of the substrate.

Also claimed are: (a) the mfr. of the semiconductor device as above, comprising: (i) forming a first dielectric film on a semiconductor substrate made of an oxide of a semiconductor which is a constituent of the substrate; (ii) performing a first heat-treatment on the substrate in a **nitriding** atmos. to **nitride** the first dielectric film, thereby converting it to a second dielectric film comprising an oxynitride of the semiconductor; and (ii) performing a second heat-treatment on the substrate in an oxidising atmos. to oxidise the substrate to produce a third dielectric film at the interface between the substrate and the second dielectric film and which comprises an oxide of the semiconductor, the third dielectric film being **thicker** than the second dielectric film, and the second and third dielectric films constituting a two-level structured insulator; (b) another **method** for mfg. the semiconductor device as above, in which a first heat-treatment of a substrate in a **nitriding** atmos. produces a first dielectric film, composed of a **nitride**, and a second heat-treatment on the substrate in an oxidising atmos. produces an oxide film at the interface between the substrate and the first dielectric film, the second dielectric film being **thicker** than the first dielectric film, and the second and third dielectric films constituting a two-level structured insulator; (c) a third **method** for mfg. the semiconductor device as above, in which a first oxide dielectric on a semiconductor substrate is subjected to a first heat-treatment to form a second dielectric comprising an oxynitride adjacent to the substrate and then to a second heat-treatment to form a third dielectric comprising an oxide at the interface between second dielectric and the substrate, followed by etching the top of the first dielectric film until its **thickness** is equal to a specified **value**, the first, second and third dielectric films constituting a three-level structured insulator; and (d) a fourth **method** for mfg. the semiconductor

device as above, in which the first dielectric film is etched away entirely to expose the second dielectric, the second and third dielectric films constituting a two-level structured insulator.

USE - Useful in the semiconductor device mfr., esp. for forming a **gate** insulator of a MOS semiconductor device.

ADVANTAGE - The **method** and structure prevent impurity atoms from diffusing into the insulator, in partic. it avoids impurities from diffusing out of a **gate** electrode into the **gate** insulator of an MOS structure.

Dwg.3/11

FS CPI EPI

FA AB; GI

MC CPI: L04-C12; L04-C16

L151 ANSWER 6 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2001-256994 [26] WPIX
DNN N2001-183245 DNC C2001-077349
TI Incorporation of **nitrogen**-based gas in polysilicon **gate** re-oxidation to improve hot carrier performance.
DC L03 U11
IN LIANG, V; MOSLEHI, B; RUBIN, M; LAPARRA, O; YEH, E
PA (VLSI-N) VLSI TECHNOLOGY INC; (PHIG) KONINK PHILIPS ELECTRONICS NV; (PHIG) PHILIPS SEMICONDUCTORS INC
CYC 24
PI US 6211045 B1 20010403 (200126)* 6p H01L021-4763
WO 2001041200 A1 20010607 (200133) EN H01L021-28 <--
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: CN JP KR
EP 1186010 A1 20020313 (200225) EN H01L021-28 <--
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU NL PT SE TR
JP 2003517729 W 20030527 (200344) 15p H01L029-78 <--
ADT US 6211045 B1 US 1999-452291 19991130; WO 2001041200 A1 WO 2000-US31855 20001118; EP 1186010 A1 EP 2000-992188 20001118, WO 2000-US31855 20001118; JP 2003517729 W WO 2000-US31855 20001118, JP 2001-542375 20001118
FDT EP 1186010 A1 Based on WO 2001041200; JP 2003517729 W Based on WO 2001041200
PRAI **US 1999-452291 19991130**
IC ICM **H01L021-28**; H01L021-4763; **H01L029-78**
ICS H01L021-336; H01L029-43; H01L029-49
AB US 6211045 B UPAB: 20010515
NOVELTY - A **nitrogen**-based gas is incorporated in polsilicon **gate** re-oxidation to improve hot carrier performance. A **gate** oxide layer is formed. **Gate** material is deposited on the **gate** oxide layer and etched to form a **gate** structure. The **gate** oxide layer and the **gate** are re-oxidised when **nitrogen**-based gas is introduced to **nitridize** re-oxidised portions of the **gate** oxide layer.
USE - Manufacture of metal-oxide-semiconductor transistor (MOST) using **nitridized gate** oxide.
ADVANTAGE - The **nitridized gate** oxide has improved hot carrier performance **compared** to standard silicon dioxide **gate**.
DESCRIPTION OF DRAWING(S) - Drawing shows reoxidation giving **thickening** of **nitridized gate** oxide layer.
**nitridized gate** oxide layer 21
buffer oxide 53
**gate** structure 42
corners of **gate** structure 51, 52
Dwg.5/5
FS CPI EPI

L123 ANSWER 25 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1998-574726 [49] WPIX
DNN N1998-447898 DNC C1998-172401
TI Manufacture of semiconductor device e.g. for MOS transistor, MIS type FET - has nitride oxidation insulating layer whose **nitrogen concentration** in **thickness** direction is different from gate insulating layer.
DC L03 U11 U12
IN HORI, M; TAMURA, N
PA (FUIT) FUJITSU LTD
CYC 3
PI JP 10256539 A 19980925 (199849)* 10p H01L029-78 <--
KR 98079644 A 19981125 (200004) H01L021-336
US 6215163 B1 20010410 (200122) H01L029-784
KR 270776 B 20001201 (200173) H01L021-336
ADT JP 10256539 A JP 1997-55275 19970310; KR 98079644 A KR 1998-1881 19980122; US 6215163 B1 US 1997-998989 19971229; KR 270776 B KR 1998-1881 19980122
FDT KR 270776 B Previous Publ. KR 98079644
PRAI **JP 1997-55275 19970310**
IC ICM H01L021-336; **H01L029-78**; H01L029-784
ICS **H01L021-318**
AB JP 10256539 A UPAB: 19981210
The method involves forming a gate insulating layer (4) containing nitride oxide on a substrate (1). A gate electrode (5) is formed on the gate insulating layer.

A pair of source-drain areas (6s,6d) are formed on the substrate at both sides of the gate electrode. A nitride oxidation insulating layer (4a) whose **nitrogen concentration** in **thickness** direction is different from the gate insulating layer covers the surface of the semiconductor substrate, including the source- drain area.

ADVANTAGE - Improves hot carrier resistance. Prevents variation. Reduces carrier trap by **nitrogen concentration** of **nitride** oxidizing zone.

Dwg.1/9
FS CPI EPI
FA AB; GI

L147 ANSWER 43 OF 53 JAPIO (C) 2003 JPO on STN
AN 1999-330263 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN HASEGAWA EIJI
PA NEC CORP
PI JP 11330263 A 19991130 Heisei
AI JP 1998-127256 (JP10127256 Heisei) 19980511
PRAI **JP 1998-127256**19980511
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
IC ICM H01L021-8234
ICS H01L027-088; H01L021-316; **H01L029-78**
AB PROBLEM TO BE SOLVED: To provide a semiconductor device and a **method** of manufacturing in which **gate** insulator films having **thickness** difference of more than a specified **value** and having without damaging reliability and by containing **nitrogen** for **gate** oxide films of small **thickness**, and a halogen-based element for **gate** oxide films of larger **thickness**.
SOLUTION: After oxide films 11 for device isolation of 400 nm are formed on a silicon substrate 10, oxide films 14 having 16 nm **thick** are formed by heat treatment. An area intending to form a **thick** insulator film is masked with photoresist 15, and **nitrogen** ions having a mass number of 14 are implanted to form a layer containing **nitrogen**. Then, an area intending to form a thin insulator film is masked with photoresist 17, and fluorine ions having a mass number of 19 are implanted to form a layer containing fluorine. The photoresist 17 is peeled off, oxide films 14 are removed, and the substrate is heat-treated to form a thin **gate** insulator film 12 having 3 nm **thick** and doped with **nitrogen** elements and a **thick** **gate** insulator film 13 having 8 nm **thick** and doped with fluorine elements. In place of fluorine, halogen-based elements representing chlorine may be used. As stated above, insulator films having **thickness** difference of more than 3 nm can be manufactured on a substrate with a single oxidizing heat-treatment while keeping the reliability and the insulation.

L123 ANSWER 23 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1999-333194 [28] WPIX
CR 2002-224448 [66]
DNN N1999-250824 DNC C1999-098470
TI Dielectric **gate** forming method for MOSFET - involves exposing semiconductor substrate to oxygen and **nitrogen** content gases to **predetermined** period to form oxy **nitride gate** dielectric layers.
DC L03 U11 U12
IN HEGDE, R I; O'MEARA, D; TOBIN, P J; TSENG, H; WANG, V
PA (MOTI) MOTOROLA INC
CYC 4
PI JP 11121453 A 19990430 (199928)* 17p H01L021-318 <--
US 5972804 A 19991026 (199952) H01L021-285
KR 99023305 A 19990325 (200024) H01L021-3205
TW 408431 A 20001011 (200116) H01L021-76
ADT JP 11121453 A JP 1998-231211 19980803; US 5972804 A CIP of US 1997-906509 19970805, US 1997-963436 19971103; KR 99023305 A KR 1998-31471 19980803; TW 408431 A TW 1998-111051 19980708
PRAI **US 1997-963436 19971103; US 1997-906509 19970805**
IC ICM H01L021-285; **H01L021-318**; H01L021-3205; H01L021-76
ICS **H01L029-78**
AB JP 11121453 A UPAB: 20020502
NOVELTY - A semiconductor substrate is exposed to **nitrogen** content gas for **predetermined** period and then to oxygen content gas. Oxy **nitride gate** dielectric films with ratio of oxygen and **nitrogen** along **thickness** of dielectric layers varying with time are formed.
USE - For MOSFET in integrated circuits.
Dwg.2/20
FS CPI EPI
FA AB; GI
MC CPI: L04-E01B1
EPI: **U11-C05B5**; U12-D02A; U12-Q

L147 ANSWER 25 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:333059 HCAPLUS
DN 135:130121
TI Approaching the limit for quantitative SIMS **measurement** of **ultra-thin** nitrided SiO2 films
AU Novak, S. W.; Bekos, E. J.; Marino, J. W.
CS Evans East, East Windsor, NJ, 08520, USA
SO Applied Surface Science (2001), 175-176, 678-684
CODEN: ASUSEE; ISSN: 0169-4332
PB Elsevier Science B.V.
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB As the demands of device performance force **gate** oxide **thicknesses** to 2 nm and less, more and more pressure is placed on conventional characterization techniques to **measure** such thin films. Although SIMS has been utilized to accurately **measure** **ultra-thin** nitrided **oxide layers** for years, we are approaching the limit at which quant. **measurements** can be made, simply because SIMS is a sputtering **process.** **Measurements** at a very low beam energies (300-1000 eV) and incidence angles (60-80.degree.) indicate ion mixing depths significantly less than 1 nm can be achieved, with the angle of incidence being more important than the beam energy in improving depth resoln. Despite these limitations, we have achieved excellent agreement between SIMS and XPS for **measurements** of N areal d. in 1.7-2.4 nm thick films. Because the ion mixing depth is significantly less than the **film thickness**, SIMS can give both the distribution and **amt.** of **N** within these thin layers.
ST nitrided silica film secondary ion mass spectrometry

4/9/1
DIALOG(R)File 2:INSPEC


7542054 INSPEC Abstract Number: A2003-07-0775-002, B2003-04-7320C-011
Title: In situ fault detection and thickness metrology using quadrupole mass spectrometry
Author(s): Rying, E.A.; Bilbro, G.L.; Ozturk, M.C.; Lu, J.C.
Author Affiliation: Dept. of Electr. & Comput. Eng., North Carolina State Univ., Raleigh, NC, USA
Conference Title: Fundamental Gas-Phase and Surface Chemistry of Vapor-Phase Deposition II and Process Control, Diagnostics, and Modeling in Semiconductor Manufacturing IV. Proceedings of the International Symposia (Electrochemical Society Proceedings Vol.2001-130 p.199-206
Editor(s): Swihart, M.T.; Allendorf, M.D.; Mevyappan, M.
Publisher: Electrochemical Society, Pennington, NJ, USA
Publication Date: 2001 Country of Publication: USA ix+508 pp.
ISBN: 1 56677 319 9 Material Identity Number: XX-2002-03058
Conference Title: Fundamental Gas-Phase and Surface Chemistry of Vapor-Phase Deposition II and Process Control, Diagnostics, and Modeling in Semiconductor Manufacturing IV. Proceedings of the International Symposia
Conference Date: 2001 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: This paper reports on an in situ sensing methodology that is applicable to thickness metrology of ultra-thin stacked oxide-nitride **gate** dielectrics and selective silicon epitaxy. The method is also applicable to selectivity loss detection during selective silicon epitaxy. In this technique, ionized molecular hydrogen (H/sub 2//sup +/) signals are collected in real-time using a quadrupole mass spectrometer (QMS) sensor and are analyzed using modern signal processing techniques. These techniques facilitate the extraction of the time-integrated hydrogen (H/sub 2//sup +/) intensity, which correlates very well with oxide (R/sup 2/=0.91), nitride (R/sup 2/=0.94) and polysilicon (R/sup 2/=0.91) film thicknesses as determined ex situ using spectroscopic ellipsometry. In selective silicon epitaxy, an inflection point in the H/sub 2//sup +/ signals was predominantly observed when undesired silicon nucleation occurred on the surrounding insulator. This change in the concavity of the hydrogen signal can be used during manufacturing as a selectivity-loss fault detector. The authors expect the methodology presented in this paper to be readily transferable to other process chemistries, especially those involving the deposition of high-k films. (13 Refs)
Subfile: A B
Descriptors: chemical vapour deposition; fault diagnosis; mass spectrometer applications; mass spectroscopy; nonelectric sensing devices; process monitoring; rapid thermal processing; **thickness measurement**; vapour phase epitaxial growth
Chemical Indexing:
H2 el - H el (Elements - 1)
SiO2-Si3N4 int - Si3N4 int - SiO2 int - Si3 int - N4 int - O2 int - Si int - **N** int - **O** int - Si3N4 bin - SiO2 bin - Si3 bin - N4 bin - O2 bin - Si bin - **N** bin - **O** bin (Elements - 2,2,3)
Si sur - Si el (Elements - 1)

L30 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:526770 HCAPLUS
DN 135:234473
TI X-ray photoelectron spectroscopy of gate-quality silicon oxynitride films produced by annealing plasma-nitrided Si(100) in nitrous oxide
AU Chen, H.-W.; Landheer, D.; Chao, T.-S.; Hulse, J. E.; Huang, T.-Y.
CS Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu, 300, Taiwan
SO Journal of the Electrochemical Society (2001), 148(7), F140-F147
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB Ultrathin silicon oxynitride films with **thickness** in the range of 1.8-3.5 nm have been produced on Si(100) by nitridation of an NO-oxidized surface with an ECR plasma source. The films were annealed in N2O at 950.degree. for times up to 60 s and formed into Al-gated capacitors for capacitance-voltage (CV) and current-voltage anal. The rapid annealing increases the oxygen content of the films but results in capacitors with excellent elec. properties. For a plasma oxynitride with equiv. oxide **thickness**, teq = 1.8 nm, current redns. of .apprx.20 over that for SiO2 films have been obtained for gate voltages in the range 1-1.5 V. For comparison, the **thickness** of the oxynitrides was obtained by XPS of the Si 2p, N 1s, and O 1s photoelectrons. By analyzing the yield from thick silicon dioxide and silicon nitride films, the electron escape depth in silicon nitride was estd. to be 1.7 nm for the Si 2p electrons. By correcting the measurements of the oxygen/nitrogen concn. ratio obtained from the O 1s and N 1s XPS peaks, and calcg. the dielec. const. with a Bruggeman effective medium approxn., the equiv. oxide **thickness** was calcd. Agreement to .apprx.0.2 nm was obtained with teq detd. by the CV anal. Information obtained from the XPS anal. can also give information about bonding configurations and possible errors due to nonuniform stoichiometry as a **function** of depth.

4/9/3
DIALOG(R)File 2:INSPEC


7248984 INSPEC Abstract Number: A2002-11-6855-075, B2002-06-2530F-002
Title: Characterization of ultra-thin **gate** dielectrics using combined grazing x-ray reflectance and spectroscopic ellipsometry
Author(s): Boher, P.; Piel, J.-P.; Evrard, P.; Defranoux, C.; Stehle, J.-L.
Author Affiliation: SOPRA S.A, Bois-Colombes, France
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4405 p.44-55
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2001 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2001)4405L.44:CUTG;1-D
Material Identity Number: C574-2001-261
U.S. Copyright Clearance Center Code: 0277-786X/01/$15.00
Conference Title: Process and Equipment Control in Microelectronic Manufacturing II
Conference Sponsor: SPIE; Scottish Enterprise
Conference Date: 30-31 May 2001 Conference Location: Edinburgh, UK
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Precise characterization of high k **gate** dielectrics becomes a challenging task due to the thinness (<3-4 nm) required for next generation integrated circuits. Conventional techniques such as spectroscopic ellipsometry in the visible range become difficult to use alone because of the correlation between thickness and optical indices. To overcome this problem the following strategy is applied. First, grazing x-ray reflectance is used to extract the different layer thickness using a simple model. Second, spectroscopic ellipsometry is applied and the results fitted with the structural models deduced from the x-ray results. Thus, a precise structural model is built which can takes into account the interface and surface factors that become critical for this range of thickness. The approach is applied to various types of oxide nitride **gate** dielectrics and ZrO/sub 2/ films. In the first case, the nitrogen content of the films can be precisely determined and also the inhomogeneity in depth of the layers in some cases. Interface problems can also be detected on ZrO/sub 2/ films. Results are compared to x-ray photo-emission measurement in some cases. (13 Refs)
Subfile: A B
Descriptors: dielectric thin films; ellipsometry; silicon compounds; surface topography; **thickness measurement**; visible spectra; X-ray reflection; zirconium compounds
Chemical Indexing:
SiON int - Si int - **N** int - **O** int - SiON ss - Si ss - **N** ss - **O** ss (Elements - 3)
ZrO2 int - O2 int - Zr int - **O** int - ZrO2 bin - O2 bin - Zr bin - **O** bin (Elements - 2)
Numerical Indexing: size 3.0E-09 to 4.0E-09 m

4/9/5
DIALOG(R)File 2:INSPEC


7170036 INSPEC Abstract Number: A2002-06-0630C-006, B2002-03-7320C-022
Title: Characterization of ultrathin dielectric films buried under poly-Si electrodes using X-ray reflectivity
Author(s): Park, C.; Ji, S.; Lee, K.-B.; Youn, S.B.; Park, J.-C.; Choi, H.
Author Affiliation: Dept. of Phys., Pohang Univ. of Sci. & Technol., South Korea
Journal: AIP Conference Proceedings Conference Title: AIP Conf. Proc. (USA) no.550 p.605-9
Publisher: AIP,
Publication Date: 2001 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
SICI: 0094-243X(2001)550L.605:CUDF;1-V
Material Identity Number: A210-2001-005
U.S. Copyright Clearance Center Code: 0094-243X/01/$18.00
Conference Title: Characterization and Metrology for ULSI Technology 2000. International Conference
Conference Sponsor: NIST; Int. Semicond. Manuf. Technol.; Nat. Sci. Found.; American Vacuum Soc.; et al
Conference Date: 26-29 June 2000 Conference Location: Gaithersburg, MD, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Probing of deep buried **gate** dielectric thin films under poly-Si electrode capping layers by X-ray reflectivity using synchrotron radiation has been demonstrated. The structural variation in the **gate** insulator was observed sensitively and the density depth profiles were obtained with a depth resolution of less than 4AA. The structural parameters were evaluated quantitatively from a discrete-layers model using the modified Parratt recursive formalism, provided that the real interfaces could be represented by a continuous refractive index profile. The depth profiles from the discrete-layers model which considers the interfacial roughness were compared to those from the continuous-media model within the experimental limit that doesn't include interfacial roughness. Consistency was so satisfactory that we could suggest X-ray reflectivity to be a reliable measurement of the thickness of ultrathin dielectric films and to be useful for the offline characterizations of structural variation from thermal processes. (11 Refs)
Subfile: A B
Descriptors: buried layers; density; dielectric thin films; interface roughness; synchrotron radiation; **thickness measurement**; X-ray reflection
Chemical Indexing:
Si sur - Si el (Elements - 1)
Si int - Si el (Elements - 1)
SiON int - Si int - **N** int - **O** int - SiON ss - Si ss - **N** ss - **O** ss (Elements - 3)

4/9/13
DIALOG(R)File 2:INSPEC


5436050 INSPEC Abstract Number: B9701-2560R-027
Title: 25 AA **gate** oxide without boron penetration for 0.25 and 0.3-mu m PMOSFETs
Author(s): Liu, C.T.; Ma, Y.; Cheung, K.P.; Chang, C.P.; Fritzinger, L.; Becerro, J.; Luftman, H.; Vaidya, H.M.; Colonell, J.I.; Kamgar, A.; Minor, J.F.; Murray, R.G.; Lai, W.Y.C.; Pai, C.S.; Hillenius, S.J.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Conference Title: 1996 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.96CH35944) p.18-19
Publisher: Widerkehr & Associates, Gaithersburg, MD, USA
Publication Date: 1996 Country of Publication: USA xv+247 pp.
ISBN: 0 7803 3342 X Material Identity Number: XX96-01867
U.S. Copyright Clearance Center Code: 0 7803 3342 X/96/$5.00
Conference Title: 1996 Symposium on VLSI Technology. Digest of Technical Papers
Conference Date: 11-13 June 1996 Conference Location: Honolulu, HI, USA
Availability: IEEE, 445 Hoes Lane, Piscataway, NJ 08855, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: Very thin **gate** oxides are necessary for small CMOS transistors. However, one major challenge is boron penetration through the thin **gate** oxides in surface-channel PMOSFETs. Other difficulties include low breakdown voltage, thickness variation control, and device reliabilities. In this work, nitrogen was implanted in the substrate before growing thin **gate** oxides. 0.25- mu m and 0.30- mu m surface-channel PMOSFETs were then fabricated. New results on oxide properties and device characteristics are observed. (1 Refs)
Subfile: B
Descriptors: boron; ion implantation; MOSFET; nitrogen; oxidation
Identifiers: **gate** oxide; boron penetration; CMOS transistor; surface-channel PMOSFET; **thickness control**; reliability; breakdown voltage; nitrogen implantation; fabrication; 0.25 micron; 0.30 micron; Si:N-SiO/sub 2/:B
Chemical Indexing:
Si:**N**-SiO2:B int - SiO2:B int - Si:**N** int - SiO2 int - O2 int - Si int - B int - **N** int - **O** int - SiO2:B ss - SiO2 ss - O2 ss - Si ss - B ss - **O** ss - Si:**N** bin - SiO2 bin - O2 bin - Si bin - **N** bin - **O** bin - Si el - B el - **N** el - B dop - **N** dop
(Elements - 1,1,2,2,1,3,4)

4/9/12
DIALOG(R)File 2:INSPEC


5622396 INSPEC Abstract Number: B9708-2560R-021
Title: High quality thin **gate** dielectric using ECR N/sub 2/O-plasma for future poly-Si TFT applications
Author(s): Lee, J.-W.; Lee, N.-I.; Han, C.-H.
Author Affiliation: Dept. of Electr. Eng., Korea Adv. Inst. of Sci. & Technol., Seoul, South Korea
Conference Title: Proceedings of the Third Symposium on Thin Film Transistor Technologies p.79-88
Editor(s): Kuo, Y.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA xil+404 pp.
Material Identity Number: XX96-02895
Conference Title: Proceedings of Thin Film Transistor Technologies III (ISBN 1 56677 173 0)
Conference Sponsor: Electrochem. Soc
Conference Date: 7-11 Oct. 1996 Conference Location: San Antonio, TX, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Electron cyclotron resonance (ECR) nitrous oxide (N/sub 2/O) plasma oxidation has been investigated as a thin **gate** oxide growth process. Although the N/sub 2/O-plasma oxidation is performed at low temperature (<or=400 degrees C), it is found that nitrogen can be successfully piled-up at the Si-SiO/sub 2/ interface and that incorporated nitrogen atoms are tightly bound with silicon atoms with a binding energy of 397.8 eV. N/sub 2/O-plasma oxidation has good thickness controllability with self-limiting oxidation resulting from a nitrogen-rich layer at the interface. Thin N/sub 2/O-plasma oxide grown on polysilicon film exhibits a smooth and uniform interface and shows good electrical characteristics. The fabricated poly-Si TFT with N/sub 2/O-plasma oxidation shows higher performance than that with thermal oxide. It is believed that the passivation effects and smooth interface are responsible for the improved characteristics. (18 Refs)
Subfile: B
Identifiers: thin **gate** dielectric; ECR N/sub 2/O-plasma; poly-Si TFT applications; electron cyclotron resonance N/sub 2/O plasma oxidation; thin **gate** oxide growth; N/sub 2/O-plasma oxidation; nitrogen pile-up; Si-SiO/sub 2/ interface; incorporated nitrogen atoms; silicon atoms; binding energy; **thickness control**; self-limiting oxidation;
Chemical Indexing:
Si-SiO2 int - SiO2 int - O2 int - Si int - **O** int - SiO2 bin - O2 bin - Si bin - **O** bin - Si el (Elements - 1,2,2)
N2O bin - N2 bin - **N** bin - **O** bin (Elements - 2)
Si:**N**-SiO2 int - Si:**N** int - SiO2 int - O2 int - Si int - **N** int - **O** int - Si:**N** bin - SiO2 bin - O2 bin - Si bin - **N** bin - **O** bin - Si el - **N** el - **N** dop (Elements - 1,1,2,2,3)

4/9/11
DIALOG(R)File 2:INSPEC


5981975 INSPEC Abstract Number: B9809-1265D-022
Title: A new SONOS memory using source-side injection for programming
Author(s): Kuo-Tung Chang; Wei-Ming Chen; Swift, C.; Higman, J.M.; Paulson, W.M.; Ko-Min Chang
Author Affiliation: Semicond. Technol. Lab., Motorola Inc., Austin, TX, USA
Journal: IEEE Electron Device Letters vol.19, no.7 p.253-5
Publisher: IEEE,
Publication Date: July 1998 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199807)19:7L.253:SMUS;1-7
Material Identity Number: I338-98007
U.S. Copyright Clearance Center Code: 0741-3106/98/$10.00
Document Number: S0741-3106(98)04777-6
Language: English Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P)
Abstract: We reported a new polysilicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory using channel hot electron injection for high-speed programming. For the first time, we demonstrated that source-side injection technique, which is commonly used in floating **gate** nonvolatile memories for its high programming efficiency, can also be used in a SONOS device for achieving high-speed programming. Erase of the device is achieved by tunneling of electrons through the thin top oxide of the ONO charge storage stack. Since the thin top oxide is grown from the nitride layer, the self-saturated nature of the oxidation allows better thickness control. Endurance characteristics indicates that quality of the thin top grown from nitride is as good as the tunnel oxide grown from the silicon substrate. By increasing the top oxide thickness, it is possible to achieve ten years of retention requirement. The self-aligned sidewall **gate** structure allows small cell size for high density applications. (10 Refs)
Identifiers: SONOS memory; source-side injection; programming; polysilicon-oxide-nitride-oxide-silicon nonvolatile memory; channel hot electron injection; high-speed programming; source-side injection technique ; erase; tunneling; thin top oxide; ONO charge storage stack; self-saturated oxidation; **thickness control**; endurance
Chemical Indexing:
Si-SiO2-Si3N4-SiO2-Si int - Si3N4 int - SiO2 int - Si3 int - N4 int - O2 int - Si int - **N** int - **O** int - Si3N4 bin - SiO2 bin - Si3 bin - N4 bin - O2 bin - Si bin - **N** bin - **O** bin - Si el (Elements - 1,2,2,2,1,3)

4/9/10
DIALOG(R)File 2:INSPEC


6010766 INSPEC Abstract Number: A9819-7340Q-011, B9810-2530F-011
Title: Ultrathin MOS **gate** insulators: surface preparation, growth, and interface control
Author(s): Nishioka, Y.; Komeda, T.; Namba, K.; Matsumura, M.; Sakoda, T.; Kubota, T.; Yamashita, Y.; Kobayashi, H.
Author Affiliation: Tsukuba Res. & Dev. Center Ltd., Ibaraki, Japan
Conference Title: Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films p.347-62
Editor(s): Deen, M.J.; Brown, W.D.; Sundaram, K.B.; Raider, S.I.
Publisher: Electochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA xiii+588 pp.
ISBN: 1 56677 137 4 Material Identity Number: XX98-00730
Conference Title: Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films
Conference Date: 4-9 May 1997 Conference Location: Montreal, Que., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: This paper overviews our several research highlights on Si surfaces and ultrathin **gate** insulators. They are on layer-by-layer etching of Si(111) surfaces with diluted oxygen, Si surface roughness observations after oxidation, nearly temperature independent growth of ultrathin oxynitrides in an N/sub 2/O ambient, annealing effects on ultrathin oxides associated with their interface density change, thickness measurements using a self-assembled-monolayer, and a new method to measure the MOS interface trap density utilizing XPS. (37 Refs)
Subfile: A B
Descriptors: annealing; electron traps; elemental semiconductors; etching; interface states; MIS structures; monolayers; nitridation; oxidation; silicon; silicon compounds; surface topography; **thickness measurement**; X-ray photoelectron spectra
Chemical Indexing:
Si-SiO2 int - SiO2 int - O2 int - Si int - **O** int - SiO2 bin - O2 bin - Si bin - **O** bin - Si el (Elements - 1,2,2)
Si sur - Si el (Elements - 1)
Si-SiON int - SiON int - Si int - **N** int - **O** int - SiON ss - Si ss - **N** ss - **O** ss - Si el (Elements - 1,3,3)

4/9/9
DIALOG(R)File 2:INSPEC


6326689 INSPEC Abstract Number: A1999-19-8115H-005, B1999-10-0520F-005
Title: Process sensing and metrology in **gate** oxide growth by rapid thermal chemical vapor deposition from SiH/sub 4/ and N/sub 2/O
Author(s): Guangquan Lu; Tedder, L.L.; Rubloff, G.W.
Author Affiliation: NSF Eng. Res. Center for Adv. Electron. Mater. Process., North Carolina State Univ., Raleigh, NC, USA
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) vol.17, no.4 p.1417-23
Publisher: AIP for American Vacuum Soc,
Publication Date: July 1999 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
SICI: 0734-211X(199907)17:4L.1417:PSMG;1-6
Material Identity Number: C067-1999-004
U.S. Copyright Clearance Center Code: 0734-211X/99/17(4)/1417(7)/$15.00
Document Number: S0734-211X(99)07704-5
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: Active sampling mass spectrometry has been used for process sensing in **gate** oxide growth by rapid thermal chemical vapor deposition from SiH/sub 4/ and N/sub 2/O. Equipment and process behavior throughout the short process cycle were revealed in the detailed time-dependent changes of downstream mass spectroscopic signals. A H/sub 2/ reaction product was clearly identified during SiO/sub 2/ deposition for SiH/sub 4//N/sub 2/O ratios of 0.5%-2.0% at 5 Torr total pressure and in the temperature range 750-850 degrees C. No H/sub 2/O product was observed, suggesting that the process is dominated by a two-step reaction involving SiH/sub 4/ pyrolysis and subsequent N/sub 2/O oxidation of the deposited Si to form SiO/sub 2/. The evolution of the H/sub 2/ product signal during a process was then used as a process indicator. The integrated H/sub 2/ signal was found linearly proportional to the deposited oxide thickness, providing the basis for real-time, noninvasive thickness metrology applications. This work demonstrates that properly configured real-time mass spectrometry is capable of providing not only time-dependent chemical information about system behavior, but also quantitative metrology for the film deposition process. (17 Refs)
Subfile: A B
Descriptors: chemical vapour deposition; insulating thin films; mass spectroscopic chemical analysis; oxidation; process monitoring; pyrolysis; rapid thermal processing; silicon compounds; **thickness measurement**
Chemical Indexing:
SiO2 int - O2 int - Si int - **O** int - SiO2 bin - O2 bin - Si bin - **O** bin (Elements - 2)
Si sur - Si el (Elements - 1)
SiH4N2O ss - H4 ss - N2 ss - Si ss - H ss - **N** ss - **O** ss (Elements - 4)
SiH4 bin - H4 bin - Si bin - H bin (Elements - 2)
N2O bin - N2 bin - **N** bin - **O** bin (Elements - 2)
Numerical Indexing: pressure 6.7E+02 Pa; temperature 1.02E+03 to 1.12E+03 K

4/9/8
DIALOG(R)File 2:INSPEC


7169958 INSPEC Abstract Number: A2002-06-0630C-001, B2002-03-7320C-012
Title: Optical and electrical thickness measurements of alternate **gate** dielectrics: a fundamental difference
Author(s): Richter, C.A.; Nguyen, N.V.; Gusev, E.P.; Zabel, T.H.; Alers, G.B.
Author Affiliation: Semicond. Electron. Div., Nat. Inst. of Stand. & Technol., Gaithersburg, MD, USA
Journal: AIP Conference Proceedings Conference Title: AIP Conf. Proc. (USA) no.550 p.134-9
Publisher: AIP,
Publication Date: 2001 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
SICI: 0094-243X(2001)550L.134:OETM;1-8
Material Identity Number: A210-2001-005
U.S. Copyright Clearance Center Code: 0094-243X/01/$18.00
Conference Title: Characterization and Metrology for ULSI Technology 2000. International Conference
Conference Sponsor: NIST; Int. Semicond. Manuf. Technol.; Nat. Sci. Found.; American Vacuum Soc.; et al
Conference Date: 26-29 June 2000 Conference Location: Gaithersburg, MD, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: We will describe a fundamental difference between the interpretation of optical and electrical measurements of **gate** dielectric thickness. This difference has major ramifications on the characterization of, and metrology for, advanced, alternate **gate** dielectrics and **gate** dielectric stacks. The purpose of this paper is to clear up possible misunderstandings that arise when comparing the thickness of **gate** dielectrics derived from optical and electrical measurements. Oxynitride data will be used to illustrate the divergence between optical and electrical measurements of thickness for films with a permittivity near and slightly above that of SiO/sub 2/. Experimental characterization of Ta/sub 2/O/sub 5/ dielectrics will demonstrate the complementary nature of electrical and optical measurements. (14 Refs)
Subfile: A B
Descriptors: capacitance; dielectric thin films; ellipsometry; permittivity; silicon compounds; tantalum compounds; **thickness measurement**
Chemical Indexing:
SiON ss - Si ss - **N** ss - **O** ss (Elements - 3)
Ta2O5 bin - Ta2 bin - O5 bin - Ta bin - **O** bin (Elements - 2)

4/9/7
DIALOG(R)File 2:INSPEC


7169960 INSPEC Abstract Number: A2002-06-0630C-002, B2002-03-7320C-013
Title: **Gate** dielectric thickness metrology using transmission electron microscopy
Author(s): Scott, J.H.J.; Windsor, E.S.; Brady, D.; Canterbury, J.; Karamcheti, A.; Chism, W.; Diebold, A.C.
Author Affiliation: Surface & Microanalysis Sci. Div., Nat. Inst. of Stand. & Technol., Gaithersburg, MD, USA
Journal: AIP Conference Proceedings Conference Title: AIP Conf. Proc. (USA) no.550 p.144-8
Publisher: AIP,
Publication Date: 2001 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
SICI: 0094-243X(2001)550L.144:GDTM;1-W
Material Identity Number: A210-2001-005
U.S. Copyright Clearance Center Code: 0094-243X/01/$18.00
Conference Title: Characterization and Metrology for ULSI Technology 2000. International Conference
Conference Sponsor: NIST; Int. Semicond. Manuf. Technol.; Nat. Sci. Found.; American Vacuum Soc.; et al
Conference Date: 26-29 June 2000 Conference Location: Gaithersburg, MD, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Silicon oxynitride blanket films approximately 2 nm in thickness were characterized in cross section using a 300 keV TEM/STEM. High resolution imaging was used to investigate the accuracy and precision of TEM film thickness measurements and their comparability to other techniques such as spectroscopic ellipsometry, secondary ion mass spectrometry, x-ray reflectivity, x-ray photoelectron spectroscopy, and medium energy ion scattering. Silicon oxynitride films were grown by SEMATECH and were characterized by several techniques in a SEMATECH-sponsored round robin. Cross sectional TEM samples were prepared by dimpling/ion milling and HRTEM micrographs were acquired at 297 keV using an imaging energy filter and a multiscan CCD camera. Thickness measurements were performed after calibrating the magnification using a phase contrast image of the silicon substrate. Approximately 10 measurements were performed for each film, including measurements on both sides of the cross section glue line and both sides of the dimple/ion mill perforation. Statistical analysis of the HRTEM thickness measurements reveals that the expanded uncertainty of the technique (with coverage factor k=2, designed to estimate a 95% confidence interval) can be larger than 0.33 nm. (5 Refs)
Subfile: A B
Descriptors: calibration; dielectric thin films; ellipsometry; ion-surface impact; scanning-transmission electron microscopy; secondary ion mass spectra; silicon compounds; **thickness measurement**; transmission electron microscopy; X-ray photoelectron spectra; X-ray reflection
Chemical Indexing:
SiON ss - Si ss - **N** ss - **O** ss (Elements - 3)
Numerical Indexing: size 2.0E-09 m; electron volt energy 3.0E+05 eV

L123 ANSWER 18 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2000-477114 [42] WPIX
DNN N2000-355580 DNC C2000-143550
TI Oxynitride gate dielectric, especially for a semiconductor memory device, produced by silicon substrate reaction or CVD to form an oxynitride layer and back-oxidation to form an intermediate silicon dioxide layer.
DC L03 U11 U12 U13 U14
IN BUCHMANN, D; COPEL, M; VAREKAMP, P R; BUCHANAN, D A; COPEL, M W
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 6
PI DE 19963674 A1 20000720 (200042)* 9p H01L021-336
JP 2000208510 A 20000728 (200049) 8p H01L021-318 <--
CN 1261726 A 20000802 (200058) H01L021-312
KR 2000053372 A 20000825 (200121) H01L021-336
US 6245616 B1 20010612 (200135) H01L021-336
TW 454253 A 20010911 (200242) H01L021-28 <--
ADT DE 19963674 A1 DE 1999-19963674 19991229; JP 2000208510 A JP 1999-372774 19991228; CN 1261726 A CN 1999-127448 19991230; KR 2000053372 A KR 2000-52 20000103; US 6245616 B1 US 1999-226369 19990106; TW 454253 A TW 2000-100002 20000103
PRAI **US 1999-226369 19990106**
IC ICM **H01L021-28**; H01L021-312; **H01L021-318**; H01L021-336
ICS H01L021-283; H01L021-285; **H01L021-31**; H01L021-3205; **H01L021-469**; H01L021-4763; **H01L029-78**
AB DE 19963674 A UPAB: 20000905
NOVELTY - Oxynitride gate dielectric formation comprises oxynitride layer formation on a silicon substrate by reaction or CVD and back-oxidation to form an intermediate silicon dioxide layer.

DETAILED DESCRIPTION - Oxynitride gate dielectric formation in a semiconductor device comprises:

(a) contacting the upper surface of a silicon substrate with a nitrogen- and/or oxygen-containing gas at not less than 500 deg. C to form an oxynitride layer; and

(b) contacting the substrate and the layer with an oxygen- and halogen compound-containing gas to form a silicon dioxide layer between the oxynitride layer and the substrate.

INDEPENDENT CLAIMS are also included for the following:

(i) a similar process in which the oxynitride layer is formed by CVD;

(ii) a gate dielectric in a semiconductor device, comprising a SiO2 spacer layer between a silicon substrate and an oxynitride layer; and

(iii) a gate stack in a semiconductor device, comprising a silicon substrate bearing a sequence of a SiO2 spacer layer, an oxynitride layer, a SiO2 layer and a conductive gate.

USE - Especially as an oxynitride gate dielectric in a semiconductor memory device.

ADVANTAGE - Allows formation of an oxynitride gate dielectric, which has a controlled **nitrogen concentration** profile, optimum film **thickness** uniformity, Vfb and channel hot carrier reliability, and allows formation of a 90 % pure SiO2 spacer layer formed by back-oxidation of the oxynitride.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a gate stack including an oxynitride gate dielectric.

gate stack 10
silicon substrate 12
polysilicon gate 14
gate dielectric 20

Dwg.1/4
FS CPI EPI
FA AB; GI

L147 ANSWER 22 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:526770 HCAPLUS
DN 135:234473
TI X-ray photoelectron spectroscopy of gate-quality silicon **oxynitride films** produced by annealing plasma-nitrided Si(100) in nitrous oxide
AU Chen, H.-W.; Landheer, D.; Chao, T.-S.; Hulse, J. E.; Huang, T.-Y.
CS Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu, 300, Taiwan
SO Journal of the Electrochemical Society (2001), 148(7), F140-F147
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB **Ultrathin** silicon **oxynitride films** with **thickness** in the range of 1.8-3.5 nm have been produced on Si(100) by nitridation of an NO-oxidized surface with an ECR plasma source. The films were annealed in N2O at 950.degree. for times up to 60 s and formed into Al-gated capacitors for capacitance-voltage (CV) and current-voltage anal. The rapid annealing increases the oxygen content of the films but results in capacitors with excellent elec. properties. For a plasma oxynitride with equiv. oxide **thickness**, teq = 1.8 nm, current redns. of .apprx.20 over that for SiO2 films have been obtained for gate voltages in the range 1-1.5 V. For **comparison**, the **thickness** of the oxynitrides was obtained by XPS of the Si 2p, N 1s, and O 1s photoelectrons. By analyzing the yield from thick silicon dioxide and silicon nitride films, the electron escape depth in silicon nitride was **estd**. to be 1.7 nm for the Si 2p electrons. By correcting the **measurements** of the oxygen/**nitrogen concn**. ratio obtained from the O 1s and N 1s XPS peaks, and **calcg**. the dielec. const. with a Bruggeman effective medium **approxn**., the equiv. oxide **thickness** was **calcd**. Agreement to .apprx.0.2 nm was obtained with teq detd. by the CV anal. Information obtained from the XPS anal. can also give information about bonding configurations and possible errors due to nonuniform stoichiometry as a function of depth.
ST XPS silicon **oxynitride film**; plasma nitridation

L13 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:766359 HCAPLUS
DN 136:62090
TI Dependence of electrical properties on nitrogen profile in ultrathin oxynitride gate dielectrics formed by using oxygen and nitrogen radicals
AU Watanabe, Koji; Tatsumi, Toru; Togo, Mitsuhiro; Mogami, Tohru
CS Silicon Systems Research Laboratories, NEC Corporation, Tsukuba, Ibaraki, 305-8501, Japan
SO Journal of Applied Physics (2001), 90(9), 4701-4707
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The authors studied nitrogen incorporation in ultrathin oxynitride films by using oxygen and nitrogen radicals, and studied the dependence of the elec. properties on the nitrogen profile. The nitrogen position in the films could be controlled by using different processing sequences, and the N **concn**. could be controlled at values up to 16%. In this process, the interface roughness depends on nitrogen position and nitrogen **concn**. The interface roughness tends to increase as the N position close to the SiO2-Si interface and increase with N **concn**. The results of an anal. of the elec. properties of these oxynitride films indicated that the best way to form the film was by radical nitridation after radical **oxidn**. These results show that the nitrogen position should be kept away from the SiO2-Si interface and nitrogen amt. should be localized at the surface. Using this process, the authors have successfully achieved a low-leakage 1.5 nm oxynitride (equiv. oxide thickness) and maintained good device performance. This 1.5-nm-thick oxynitride has a leakage current two orders of magnitude less than that of 1.5-nm-thick SiO2 without decreasing the drain current. Radical oxynitridation should thus be very useful in making high-quality ultrathin gate-insulator films.
ST nitrogen profile ultrathin oxynitride gate elec properties; CMOS device

L13 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:664657 HCAPLUS
DN 129:309320
TI Nitrogen profile engineering in thin gate oxides
AU Kuehne, J.; Hattangady, S.; Piccirillo, J.; Xing, G. C.; Miner, G.; Lopes, D.; Tauber, R.
CS Silicon Technology Development, Texas Instruments, Inc., Dallas, TX, 75265, USA
SO Materials Research Society Symposium Proceedings (1998), 525(Rapid Thermal and Integrated Processing VII), 181-186
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB In order to prevent boron penetration in PMOS transistors without degrading channel mobility, it is necessary to engineer the distribution of nitrogen introduced into the gate oxide. We have investigated methods of engineering this distribution using nitric oxide (NO) gas in an RTP system to thermally nitride ultrathin gate oxides. In one approach, the gate oxide is simultaneously grown and nitrided in a mixt. of nitric oxide and oxygen. For a 40 .ANG. film, SIMS depth profiling shows that this process moves the nitrogen peak into the bulk of the oxide away from the oxide silicon interface. In another approach, an 11 .ANG. chem. oxide produced by a std. pre-furnace wet clean is nitrided in NO at 800.degree. C. This film is subsequently **reoxidized** in either oxygen or steam. For an 1100.degree. C., 120 s RTP **reoxidn.** in oxygen, the final film thickness is 41 .ANG.. The nitrogen has a peak **concn.** of 5 at. % and the peak is located in the oxide 25 .ANG. from the oxide/silicon interface. Ramped voltage breakdown testing was carried out on MOS capacitors built using **reoxidized** NO nitrided films. They have breakdown characteristics that are equiv. to conventional furnace grown oxides. These films show considerable promise as gate dielecs. for CMOS technologies at geometries of 0.25 .mu.m and below.

L13 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:89616 HCAPLUS
DN 130:147914
TI X-ray photoelectron study of gate oxides and nitrides
AU Opila, R. L.; Chang, J. P.; Du, M.; Bevk, J.; Ma, Y.; Weldon, M.; Chabal, Y.; Gurevich, A.
CS Bell Laboratories, Murray Hill, NJ, 07974, USA
SO Diffusion and Defect Data--Solid State Data, Pt. B: Solid State Phenomena (1999), 65-66(Ultra Clean Processing of Silicon Surfaces), 257-260
CODEN: DDBPE8; ISSN: 1012-0394
PB Scitec Publications
DT Journal
LA English
CC 79-5 (Inorganic Analytical Chemistry)
Section cross-reference(s): 76
AB XPS can det. the elemental compn., chem. states, and Si non-stoichiometric defects as a function of depth for current gate oxides because the escape depth of the photoelectrons is comparable to the thickness of the oxide. Annealing of rapid thermally grown oxides decreases the non-stoichiometric fraction of Si as the no. of elec. defects grow. Nitrogen implanted into Si before growth of the oxide becomes incorporated at the SiO2/Si interface as the oxide grows, and the **concn**. of N can be increased by **oxidn**. in N2O. The distribution of O2 on the surface after wet chem. cleans changes as the specimen is heated, and does not form a simple overlayer.

L13 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:36077 HCAPLUS
DN 132:173935
TI Forming nitrided gate oxides by nitrogen implantation into the substrate before gate **oxidation** by RTO
AU Bauer, A. J.; Mayer, P.; Frey, L.; Haublein, V.; Ryssel, H.
CS Fraunhofer-Institut fur Integrierte Schaltungen, Erlangen, D-91058, Germany
SO Ion Implantation Technology--98, International Conference on Ion Implantation Technology Proceedings, 12th, Kyoto, June 22-26, 1998 (1999), Meeting Date 1998, Volume 1, 26-29. Editor(s): Matsuo, Jiro; Takaoka, G.; Yamada, Isao. Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 68NKAN
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB Nitrogen was implanted into a Si substrate at an energy of 20 keV with doses of 1 .times. 1013cm-2, 1 .times. 1014cm-2, and 1 .times. 1015 cm-2. After the implantation, oxides were grown by rapid thermal **oxidn**. on nitrogen implanted wafers with and without an anneal step before **oxidn**. The gate oxide growth rate and the nitrogen peak **concn**. at the SiO2/Si interface (measured by SIMS) can be controlled by the nitrogen implant dose. An implant anneal with RTP after implantation results in a significant decrease of nitrogen **concn**. at the surface or interface. However, an implant anneal also significantly decreases surface roughness and crystal defects in the substrate after N+-implantation, as shown by AFM and TEM measurements. By using nitrogen implantation with the lowest dose (1 .times. 1013 cm-2), the QBD-values can be slightly increased.

L13 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:652524 HCAPLUS
DN 135:365181
TI Nitrogen incorporation in ultrathin gate dielectrics: A comparison of He/N2O and He/N2 remote plasma processes
AU Khandelwal, Amit; Smith, Bradley C.; Lamb, H. Henry
CS Department of Chemical Engineering, North Carolina State University, Raleigh, NC, 27695, USA
SO Journal of Applied Physics (2001), 90(6), 3100-3108
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
CC 76-10 (Electric Phenomena)
AB Ultrathin Si oxynitride films grown by low-temp. remote plasma processing were examd. by online Auger electron spectroscopy and angle-resolved XPS to det. the **concn.**, spatial distribution, and chem. bonding of N. The films were grown at 300.degree. on Si(100) substrates using two radiofrequency remote plasma processes: (i) He/N2O remote plasma-assisted **oxidn.** (RPAO) and (ii) two-step remote plasma **oxidn** ./nitridation. A 5 min He/N2O RPAO process produces a 2.5 nm oxynitride film incorporating .apprx.1 monolayer of N at the Si-SiO2 interface. The interfacial N is bonded in a N-Si3 configuration, as in Si nitride (Si3N4). By comparison, a 90 s He/N2 remote plasma exposure of a 1. nm oxide (grown by 10 s He/O2 RPAO) consumes substrate Si atoms creating a 1 nm s.c. Si3N4 layer. The N areal d. obtained via the two-step process depends on the initial oxide thickness and the He/N2 remote plasma exposure time. Also, as the oxide thickness is increased (by increasing the He/O2 remote plasma exposure), the N distribution shifts away from the Si-SiO2 interface and into the oxide. More N with a tighter distribution is incorporated using He vs. Ar diln. Insight into the remote plasma chem. was provided by optical emission spectroscopy. Strong N2 1st pos. and 2nd pos. emission bands were obsd. for He/N2O and He/N2 remote plasmas indicating the presence of N2 metastables and ground-state N atoms.

L15 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:614305 HCAPLUS
DN 135:161177
TI Method to reduce gate oxide damage by using a multi-step etch process with a **predictable** premature endpoint system
IN Chhagan, Vijaikumar; Pradeep, Yelehanka R.; Tjoa, Tjin Tjin
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-4763
NCL 438584000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 6277716 | B1 | 20010821 | US 1999-425908 | 19991025 |
| | SG 84580 | A1 | 20011120 | SG 2000-1818 | 20000330 |
| PRAI | US 1999-425908 | A | 19991025 | | |

AB A method of fabricating a gate stack having an endpoint detect layer and a multi-step etch process to prevent damage to a gate dielec. layer. The special endpoint detect layer emits an endpoint signal that allows the etch chem. to be changed to a more selective polysilicon to oxide ratio to prevent damage to the gate oxide layer. The invention begins by forming a gate dielec. layer over a substrate. The authors then form an endpoint detect layer over the gate dielec. layer. A gate stack is formed over the bottom Si layer. Then a mask is formed over the gate stack. The mask defines a gate electrode. The authors etch the gate stack and the endpoint detect layer using a multi-step etch comprising at least 3 steps. In a main etch step, the gate stack and the endpoint detect layer are etched using a 1st etch chem. Upon an endpoint detection signal generated by etching the gate stack, the 1st etch step is stopped. In an endpoint detect layer etch step, the gate stack layer and the endpoint detect layer are etched using a 2nd etch chem. The endpoint etch step is stopped when an endpoint detect signal changes upon reaching the gate dielec. layer. The 2nd etch chem. has a higher selectivity from the gate dielec. layer to the gate stack layer and endpoint detect layer than the 1st etch chem. In an overetch step, using a 3rd etch chem. with a higher selectivity than the 2nd etch chem., the authors etch the endpoint detect layer without damaging the gate dielec. layer.

IT **352699-61-7**, Silicon nitride (Si0.5-0.98N0.02-0.5)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(endpoint barrier; method to reduce **gate oxide** damage by using multi-step etch process with **predictable** premature endpoint system)

L123 ANSWER 21 OF 34 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2000-442457 [38] WPIX
DNN N2000-330137 DNC C2000-134598
TI Preparation of a silicon, oxygen, and nitrogen containing film on a silicon substrate includes introducing the substrate into a rapid thermal processing system, and contacting it with nitrogen and oxygen containing components.
DC L03 U11
IN GELPEY, J; KWONG, D; MARCUS, S D
PA (MATT-N) MATTSON TECHNOLOGY INC; (STGG) STEAG RTP SYSTEMS GMBH
CYC 23
PI WO 2000036639 A1 20000622 (200038)* EN 19p H01L021-314
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR SG
US 6303520 B1 20011016 (200164) H01L021-44
EP 1157415 A1 20011128 (200201) EN H01L021-314
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
KR 2001110305 A 20011212 (200237) H01L021-314
JP 2002532900 W 20021002 (200279) 20p H01L021-31 <--
ADT WO 2000036639 A1 WO 1999-EP9452 19991203; US 6303520 B1 US 1998-212495 19981215; EP 1157415 A1 EP 1999-968789 19991203, WO 1999-EP9452 19991203; KR 2001110305 A KR 2001-707487 20010615; JP 2002532900 W WO 1999-EP9452 19991203, JP 2000-588797 19991203
FDT EP 1157415 A1 Based on WO 2000036639; JP 2002532900 W Based on WO 2000036639
PRAI **US 1998-212495 19981215**
IC ICM **H01L021-31**; H01L021-314; H01L021-44
ICS C01B021-082; C23C016-42
AB WO 200036639 A UPAB: 20000811
NOVELTY - Silicon, oxygen and nitrogen containing film is prepared on a silicon substrate by introducing the substrate into a rapid thermal processing (RTP) system. The substrate is contacted with nitrogen and oxygen containing components. The oxygen containing component has a smaller **concentration** than the **nitrogen** containing component. The temperature of the substrate is rapidly raised.

DETAILED DESCRIPTION - Preparation of silicon, oxygen and nitrogen containing film on a silicon substrate comprises introducing the substrate into the process chamber of a rapid thermal processing (RTP) system. The substrate is contacted with a first reactive gas comprising a first nitrogen containing component, and a first oxygen containing component having much smaller concentration than the first nitrogen containing component. The temperature of the substrate is rapidly raised.

An INDEPENDENT CLAIM is also included for an apparatus comprising a silicon substrate, and a film attached to the substrate. The film comprises a graded layer of silicon oxynitride, in which the oxygen content of the layer is substantial at the interface between the film and the substrate, and the nitrogen content of the layer increased with distance from the interface.

USE - For preparing silicon, oxygen, and nitrogen containing film on a silicon substrate.

ADVANTAGE - The film has an effective oxide electrical **thickness** (Teff) of 25-45 Angstrom with excellent electrical properties. It shows a leakage current density of almost two orders of magnitude less than a control silicon dioxide film. The flatband voltage is almost identical to the control oxide, which indicates that the peak **nitrogen concentration** is within the film rather than at the oxide-silicon interface, as in the case of other processes for nitriding oxides.

Dwg.0/4
TECH WO 200036639 A1UPTX: 20000811
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The first nitrogen containing component is ammonia. It is present in the reactive gas in a concentration less than 10000 ppm (preferably less than 100 ppm). The first oxygen containing component is ozone, water vapor, nitrous oxide, nitric oxide, carbon monoxide, or carbon dioxide. The second

oxygen-containing component is nitrous oxide.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method further comprises lowering the temperature of the substrate and flushing the process chamber. The substrate is contacted with a second reactive gas comprising a second oxygen containing component. The temperature of the substrate is rapidly raised to a second temperature. The substrate is irradiated with ultraviolet electromagnetic radiation during the first rapid raise of temperature.
Preferred Film: The film is less than 10 nm or less than 2 nm **thick**. Fewer than 5x1014 nitrogen atoms/cm2 or 1x1014 nitrogen atoms/cm2 are located at the substrate film interface.

FS CPI EPI
FA AB
MC CPI: L04-C12B; L04-C16; L04-C26

L41 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:805816 HCAPLUS
DN 136:93993
TI Electrical properties and modeling of ultrathin impurity-doped silicon dioxides
AU Chang, Wai-Jyh; Houng, Mau-Phon; Wang, Yeong-Her
CS Institute of Microelectronics, Department of Electrical Engineering, National Cheng-Kung University, Tainan, Taiwan
SO Journal of Applied Physics (2001), 90(10), 5171-5179
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The elec. properties of silicon dioxides doped with impurities (fluorine and/or nitrogen) were investigated. Pure silicon dioxide (SiO2), fluorine-doped silicon oxide (SiOF), nitrogen-doped silicon oxide (SiON), and nitrogen-doped SiOF (SiOFN) are the authors' choices for investigation. The oxide films were prepd. from liq.-phase-deposited fluorinated silicon oxides under O2 or N2O annealing. The leakage current as a **function** of applied voltage for impurity-doped oxides was simulated using a generalized trap-assisted tunneling (GTAT) model at moderate fields of 5-8 MV/cm. Two important parameters, trap energy level .PHI.t and trap concn. Nt, are directly derived by this model from simple current-voltage characteristics. The relations of .PHI.t and Nt on various exptl. conditions (annealing temp., time, gases, and initial oxide **thickness**) are comprehensively studied based on GTAT modelings.

L147 ANSWER 21 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:805940 HCAPLUS
DN 136:23842
TI Influence of the native **oxide layer** on the silicon surface during initial stages of nitridation
AU Markwitz, Andreas; White, Geoffrey Vaughan; Trompetter, William Joseph; Brown, Ian William Murray
CS Institute of Geological and Nuclear Sciences Ltd., Lower Hutt, N. Z.
SO Mikrochimica Acta (2001), 137(1-2), 49-56
CODEN: MIACAQ; ISSN: 0026-3672
PB Springer-Verlag Wien
DT Journal
LA English
CC 57-2 (Ceramics)
AB Thin SiO2 layers were produced by thermal oxidn. of Si wafer material. To study the effect of nitridation on the **oxide layers**, the specimens were nitrided in a furnace at high temp. Non-destructive ion beam anal. was performed to det. **changes** in the elemental concns. and depth profiles of the major components. In particular, **N** and O **concns**. were **measured** using the non-resonant nuclear reactions 14N(d,.alpha.)12C and 16O(d,p)17O, resp. To obtain depth profiles of the as-prepd. and nitrided specimens, the **samples** were **measured** with RBS and heavy ion elastic recoil detection anal. The ion beam analyses revealed an increase in **thickness** of the SiO2 **layers** with temp. The specimens nitrided at 1200.degree.C were almost free of N. Surface topol. investigations with SEM revealed concentric annular artificial patterns at the surfaces. In the center of the pattern, only silicon was **measured**. Addnl., a band consisting of Si, O, and N surrounding the pattern was discovered. The findings are in agreement with specimens prepd. at higher temps.
ST silicon wafer topol surface compn thermal oxidn nitridation
IT Nitriding

L41 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:6074 HCAPLUS
DN 136:192334
TI Influence of silicon wafer loading ambient on chemical composition and **thickness** uniformity of sub-5-nm-thick oxide films
AU Endoh, Tetsuo; Kimura, Yasutaka; Lenski, Markus; Masuoka, Fujio
CS Research Institute of Electrical Communication, Tohoku University, Aoba-ku, Sendai, 980-8577, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2001), 40(12), 7023-7028
CODEN: JAPNDE
PB Japan Society of Applied Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB The influence of silicon wafer loading conditions during the vertical furnace oxidn. process, on both the chem. compn. and **thickness** uniformity of sub-5-nm-thick oxide films is investigated by secondary ion mass spectrometry (SIMS) and XPS (XPS). Loading wafers in pure nitrogen prior to oxidn. effectively suppresses undesired peroxide growth offering controlled oxidn. in the sub-5 nm regime. However, these wafers show a pronounced **thickness** nonuniformity, which **correlates** to the nitrogen incorporated in the oxide at the central part of the wafer. Loading waters in a 1%-O2/99%-N2 ambient prior to oxidn. results in uniform oxide films. However, film **thickness** in the sub-5 nm regime is difficult to control due to an excessive peroxide growth during wafer loading. Loading wafers in a chem. inert Ar atm. or under controlled preoxidn. conditions prior to oxidn. results in uniform oxide films with controllable oxide **thickness** suitable for sub-5 nm thick oxides,.

L147 ANSWER 20 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:80232 HCAPLUS
DN 136:255062
TI Material and **process** considerations for **ultra-thin** silicon (oxy-)nitride films grown or deposited on silicon and SiO2 surfaces
AU D'Emic, C. P.; Gusev, E. P.; Chan, K.; Zabel, T.; Copel, M.; Murphy, R.; Kozlowski, P.; Newbury, J.
CS IBM- T.J. Watson Research Center, Yorktown Heights, NY, 10598, USA
SO Proceedings - Electrochemical Society (2001), 2001-7(Silicon Nitride and Silicon Dioxide Thin Insulating Films), 174-190
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
CC 76-2 (Electric Phenomena)
AB Silicon (oxy)nitride films used in the semiconductor fabrication **process** continue to be grown/deposited thinner and thinner as device dimensions continue to shrink. In this study, we have **compared** the growth kinetics, nitrogen compn. and profile, morphol. and elec. characteristics of silicon nitrides and oxy-nitrides prepd. by several techniques. These include rapid thermal (RT) **processes** such as N2O, NO, NO+O2, and NH3 (oxy)nitridations as well as **ultra-thin** LPCVD and RTCVD nitride and oxy-nitride **processes**. The **measurement** techniques used to characterize these films include: ellipsometry, nuclear reaction anal. (NRA), medium energy ion scattering (MEIS), at. force microscopy (AFM) and C-V and I-V elec. characterization of poly-**gate** capacitors. With a thorough understanding of the growth behavior, and material properties of **ultra-thin** silicon (oxy)nitride films grown by different techniques, we can tailor the **film thickness, nitrogen concn.** and profile to optimize the materials diffusion barrier and elec. properties for desired applications.
ST silicon **oxynitride film** deposition silica surface

L147 ANSWER 16 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:174086 HCAPLUS
DN 138:197308
TI Method of **monitoring** nitrogen implantation dosages in semiconductor devices
IN Yen, Chun-yao
PA Taiwan
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM G21K005-10
NCL 250492210
CC 76-14 (Electric Phenomena)

8/28/2001 priority

FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 2003042432 | A1 | 20030306 | US 2002-59714 | 20020129 |
| PRAI | TW 2001-90121169 | A | 20010828 | | |

AB The invention relates to a method of **monitoring** nitrogen implantation dosages in semiconductor devices based on the relationship between implantation dosage and the resulting **thickness** of a subsequently formed **oxide layer**. The semiconductor wafers are first implanted with various **concn**. of mol. **nitrogen**. After implantation, the implanted wafers and a non-implanted wafer are subjected to a thermal process to grow an **oxide layer**. The **thickness** of **oxide layer** on the wafers with various implantation dosages is **measured**. Because implanted nitrogen on the wafers suppresses the growth of **oxide layer**, a suppression ratio is computed from the difference in **thickness** of the **oxide layer** between the implanted and non-implanted semiconductor wafers to stand for the **thickness** variation. Then, a relation between the suppression ratio and the dosages of mol. nitrogen is developed such that a predetd. **thickness** of oxide can be grown by adjusting the implantation dosage.